Table of Content

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Description

Note

Option

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

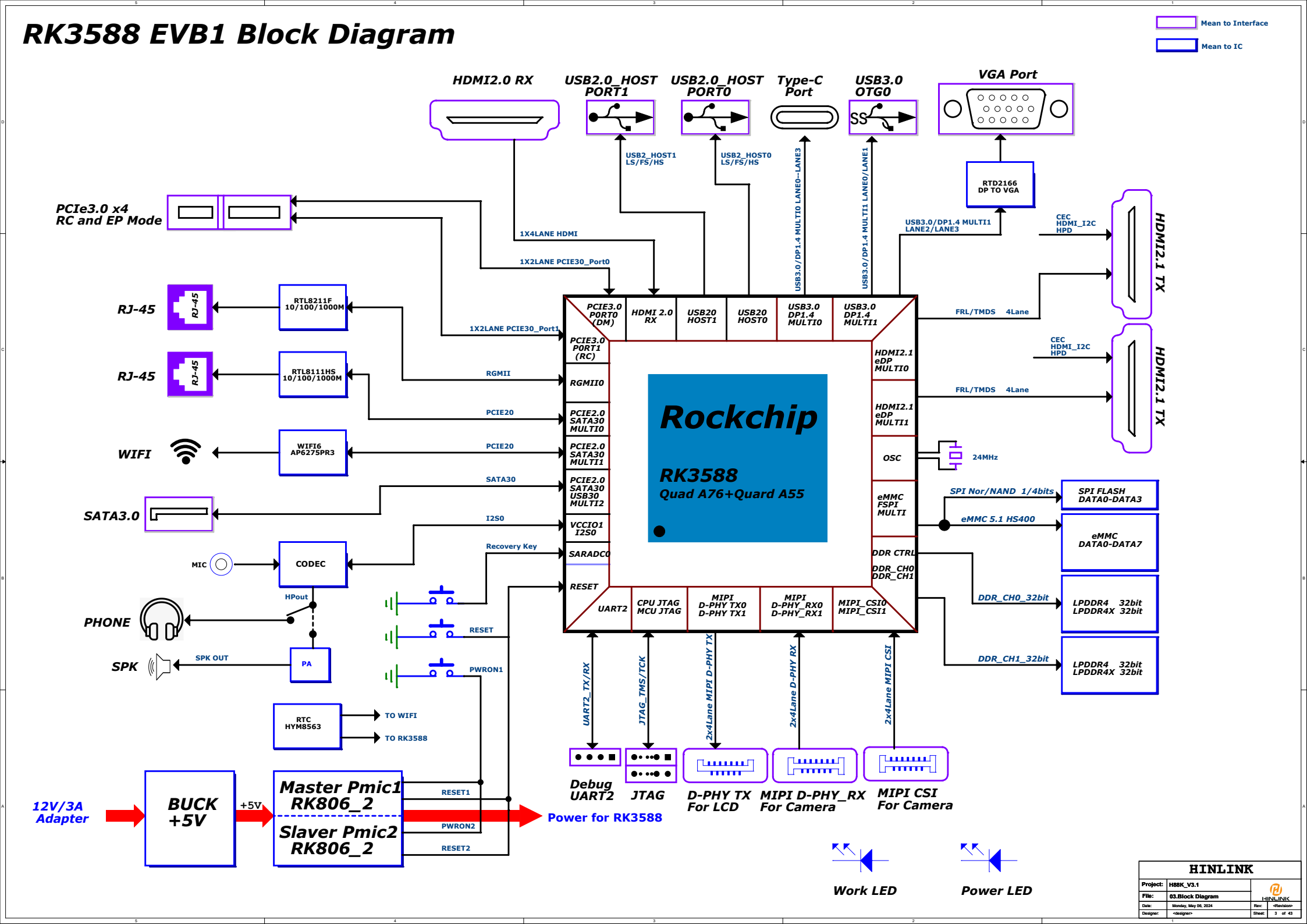
HINLINK			
Project:	H88K_V3.1	HINLINK	
File:	01.Index and Notes		
Date:	Monday, May 06, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	1 of 43

Revision History

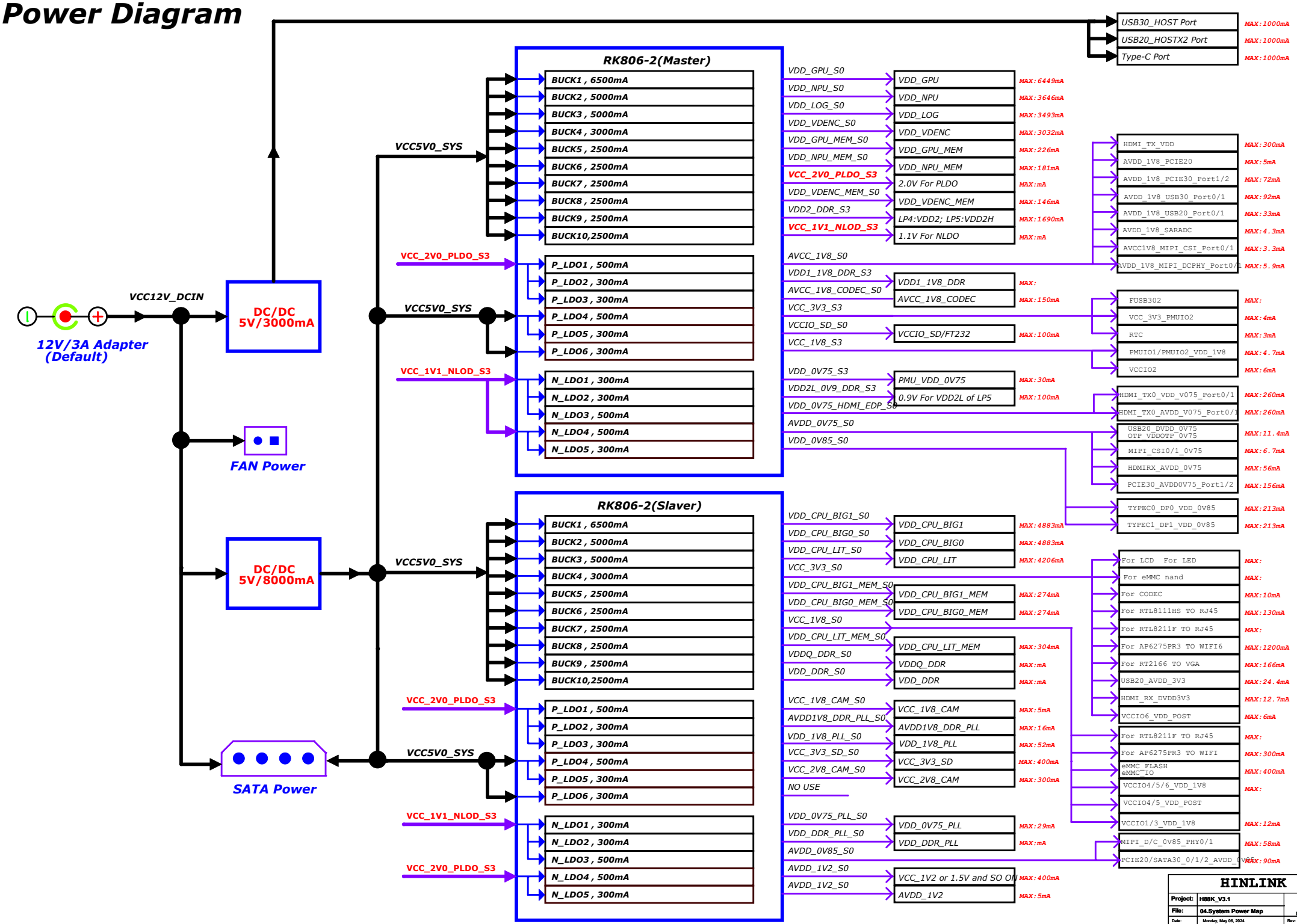
Version	Date	By	Change Dsecription	Approved
V1.0	2021-08-09	Felix.ruan	1:Revision preliminary version	

HINLINK			
Project:	H88K_V3.1	HINLINK	
File:	02.Revision History		
Date:	Monday, May 06, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	2 of 43

RK3588 EVB1 Block Diagram



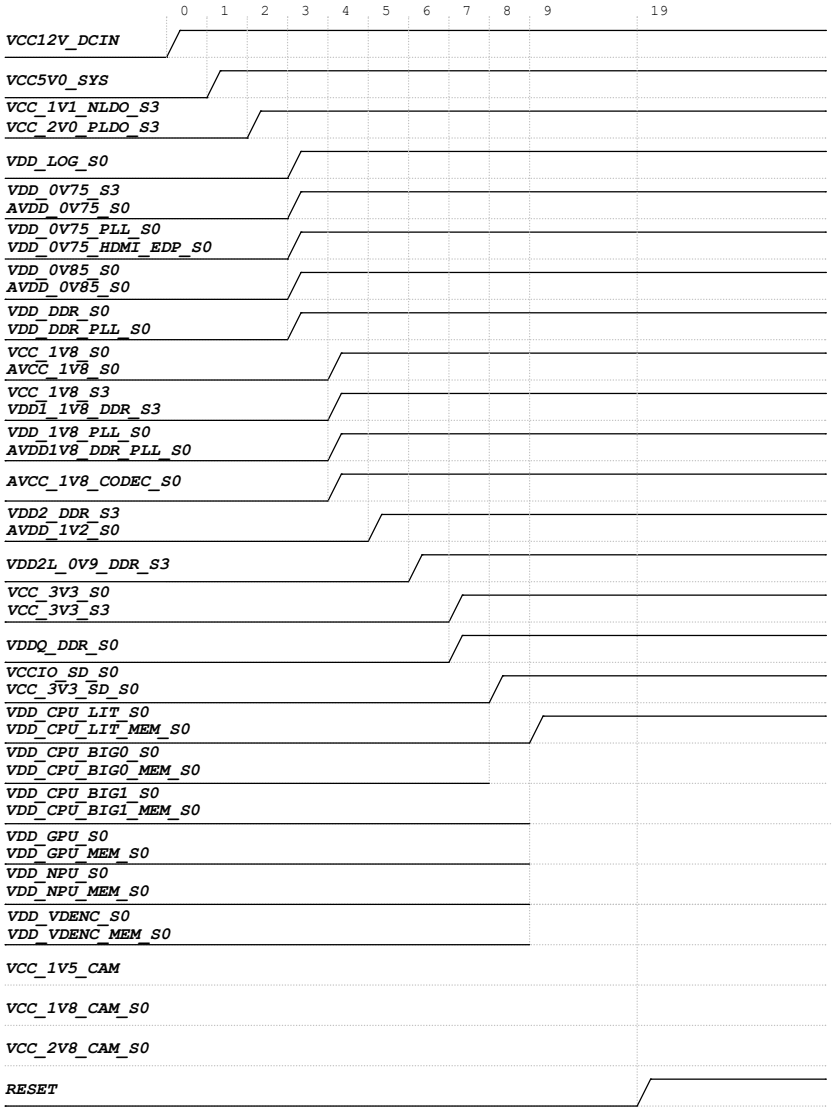
Power Diagram



Project:	H88K_V3.1
File:	04.System Power Map
Date:	Monday, May 06, 2024
Designer:	<designer>
Rev:	<Revision>
Sheet:	4 of 43

HINLINK

Power Sequence



Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC5V0_SYS	PMIC1_BUCK1	6.5A	VDD_GPU_S0		0.75V	OFF	OFF	TBD	TBD
VCC5V0_SYS	PMIC1_BUCK2	5A	VDD_NPU_S0		0.75V	OFF	OFF	TBD	TBD
VCC5V0_SYS	PMIC1_BUCK3	5A	VDD_LOG_S0		0.75V	ON	OFF	TBD	TBD
VCC5V0_SYS	PMIC1_BUCK4	3A	VDD_VDENC_S0		0.75V	OFF	OFF	TBD	TBD
VCC5V0_SYS	PMIC1_BUCK5	2.5A	VDD_GPU_MEM_S0		0.75V	OFF	OFF	TBD	TBD
VCC5V0_SYS	PMIC1_BUCK6	2.5A	VDD_NPU_MEM_S0		0.75V	OFF	OFF	TBD	TBD
VCC5V0_SYS	PMIC1_BUCK7	2.5A	VCC_2V0_PLDO_S3		2.0V	ON	ON	TBD	TBD
VCC5V0_SYS	PMIC1_BUCK8	2.5A	VDD_VDENC_MEM_S0		0.75V	OFF	OFF	TBD	TBD
VCC5V0_SYS	PMIC1_BUCK9	2.5A	VDD2_DDR_S3		1.1V	ON	ON	TBD	TBD
VCC5V0_SYS	PMIC1_BUCK10	2.5A	VCC_1V1_NLDO_S3		1.1V	ON	ON	TBD	TBD
VCC_2V0_PLDO	PMIC1_PLDO1	0.3A	AVCC_1V8_S0		1.8V	ON	OFF	TBD	TBD
	PMIC1_PLDO2	0.3A	VDD1_1V8_DDR_S3		1.8V	ON	ON	TBD	TBD
	PMIC1_PLDO3	0.5A	AVCC_1V8_CODEC_S0		1.8V	ON	OFF	TBD	TBD
VCC5V0_SYS	PMIC1_PLDO4	0.5A	VCC_3V3_S3		3.3V	ON	ON	TBD	TBD
	PMIC1_PLDO5	0.3A	VCCIO_SD_S0		3.3V	ON	OFF	TBD	TBD
VCC5V0_VCCA	PMIC1_PLDO6	0.3A	VCC_1V8_S3		1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO	PMIC1_NLDO1	0.3A	VDD_0V75_S3		0.75V	ON	ON	TBD	TBD
	PMIC1_NLDO2	0.3A	VDD2L_0V9_DDR_S3		0.9V	ON	ON	TBD	TBD
	PMIC1_NLDO3	0.5A	VDD_0V75_HDMI_EDP_S0		0.75V	ON	OFF	TBD	TBD
VCC_1V1_NLDO	PMIC1_NLDO4	0.5A	AVDD_0V75_S0		0.75V	ON	OFF	TBD	TBD
	PMIC1_NLDO5	0.3A	VDD_0V85_S0		0.85V	ON	OFF	TBD	TBD
VCC5V0_SYS	PMIC2_BUCK1	6.5A	VDD_CPU_BIG1_S0		0.75V	OFF	OFF	TBD	TBD
VCC5V0_SYS	PMIC2_BUCK2	5A	VDD_CPU_BIG0_S0		0.75V	OFF	OFF	TBD	TBD
VCC5V0_SYS	PMIC2_BUCK3	5A	VDD_CPU_LIT_S0		0.75V	ON	OFF	TBD	TBD
VCC5V0_SYS	PMIC2_BUCK4	3A	VCC_3V3_S0		3.3V	ON	OFF	TBD	TBD
VCC5V0_SYS	PMIC2_BUCK5	2.5A	VDD_CPU_BIG1_MEM_S0		0.75V	OFF	OFF	TBD	TBD
VCC5V0_SYS	PMIC2_BUCK6	2.5A	VDD_CPU_BIG0_MEM_S0		0.75V	OFF	OFF	TBD	TBD
VCC5V0_SYS	PMIC2_BUCK7	2.5A	VCC_1V8_S0		1.8V	ON	OFF	TBD	TBD
VCC5V0_SYS	PMIC2_BUCK8	2.5A	VDD_CPU_LIT_MEM_S0		0.75V	ON	OFF	TBD	TBD
VCC5V0_SYS	PMIC2_BUCK9	2.5A	VDDQ_DDR_S0		0.6V	ON	OFF	TBD	TBD
VCC5V0_SYS	PMIC2_BUCK10	2.5A	VDD_DDR_S0		0.85V	ON	OFF	TBD	TBD
VCC_2V0_PLDO	PMIC2_PLDO1	0.3A	VCC_1V8_CAM_S0		0V	OFF	OFF	TBD	TBD
	PMIC2_PLDO2	0.3A	AVDD1V8_DDR_PLL_S0		1.8V	ON	OFF	TBD	TBD
	PMIC2_PLDO3	0.5A	VDD_1V8_PLL_S0		1.8V	ON	OFF	TBD	TBD
VCC5V0_SYS	PMIC2_PLDO4	0.5A	VCC_3V3_SD_S0		3.3V	ON	OFF	TBD	TBD
	PMIC2_PLDO5	0.3A	VCC_2V8_CAM_S0		0V	OFF	OFF	TBD	TBD
VCC_1V1_NLDO	PMIC2_NLDO1	0.3A	VDD_0V75_PLL_S0		0.75V	ON	OFF	TBD	TBD
	PMIC2_NLDO2	0.3A	VDD_DDR_PLL_S0		0.85V	ON	OFF	TBD	TBD
	PMIC2_NLDO3	0.5A	AVDD_0V85_S0		0.85V	ON	OFF	TBD	TBD
VCC_2V0_PLDO	PMIC2_NLDO4	0.5A	VCC_1V2_CAM_S0		0V	OFF	OFF	TBD	TBD
	PMIC2_NLDO5	0.3A	AVDD_1V2_S0		1.2V	ON	OFF	TBD	TBD

IO Power Domain Map

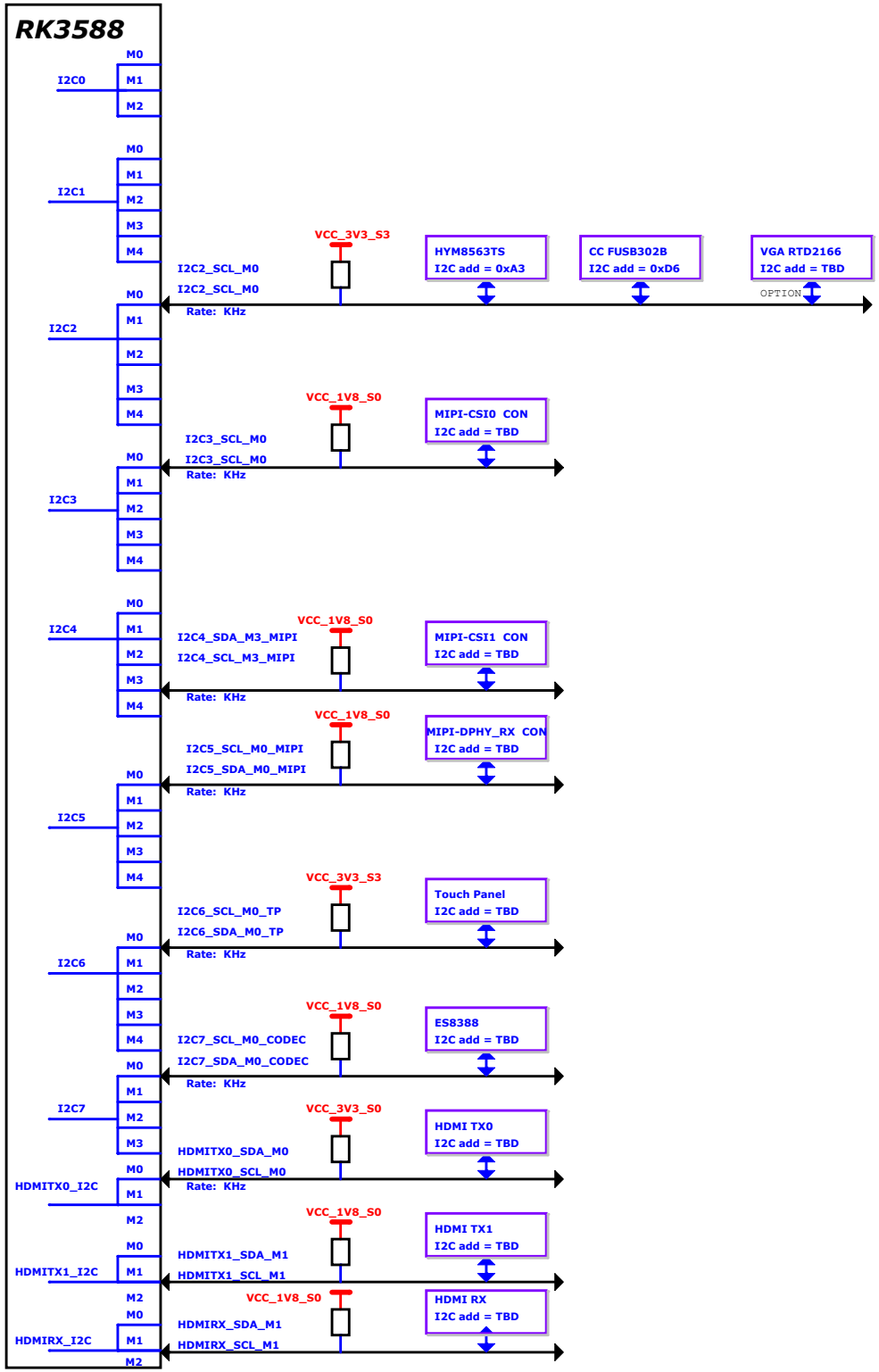
IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO1	Pin N28	1.8V Only	PMUIO1_1V8	VCC_1V8_S3	1.8V
PMUIO2	Pin R27 Pin P28	1.8V or 3.3V	PMUIO2_1V8 PMUIO2	VCC_1V8_S3 VCC_3V3_S3	3.3V
EMMCIO	Pin V26	1.8V Only	EMMCIO_1V8	VCC_1V8_S0	1.8V
VCCIO1	Pin G20	1.8V Only	VDDIO1_1V8	VCC_1V8_S0	1.8V
VCCIO2	Pin AA7 Pin Y7	1.8V or 3.3V	VDDIO2_1V8 VCCIO2	VCC_1V8_S0 VCC_1V8/3V3_S0	1.8V/3.3V
VCCIO3	Pin Y26	1.8V Only	VDDIO3_1V8	VCC_1V8_S0	1.8V
VCCIO4	Pin H20 Pin H21	1.8V or 3.3V	VDDIO4_1V8 VCCIO4	VCC_1V8_S0 VCC_1V8_S0	1.8V
VCCIO5	Pin W25 Pin W26	1.8V or 3.3V	VDDIO5_1V8 VCCIO5	VCC_1V8_S0 VCC_1V8_S0	1.8V
VCCIO6	Pin AC25 Pin AC26	1.8V or 3.3V	VDDIO6_1V8 VCCIO6	VCC_1V8_S0 VCC_3V3_S0	3.3V

IO Type	Operating Voltage
1.8V Only	VCCIO*_1V8=1.8V
1.8V or 3.3V	VCCIO*_1V8=1.8V VCCIO*=1.8V or 3.3V

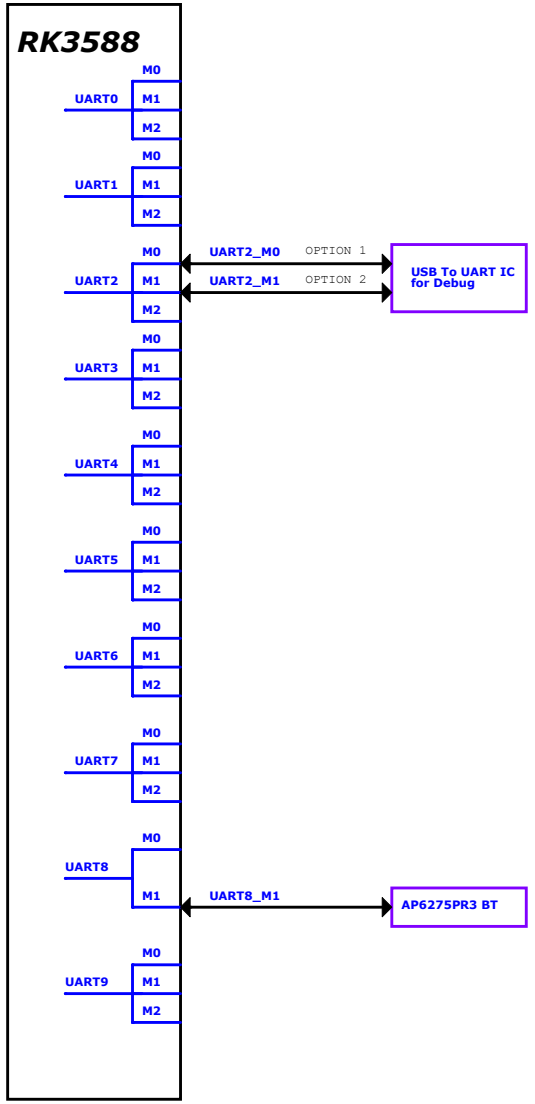
HINLINK

Project:	H88K_V3.1	HINLINK	
File:	05.Power Sequence/IO Power		
Date:	Monday, May 06, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	5 of 43

I2C MAP



UART MAP



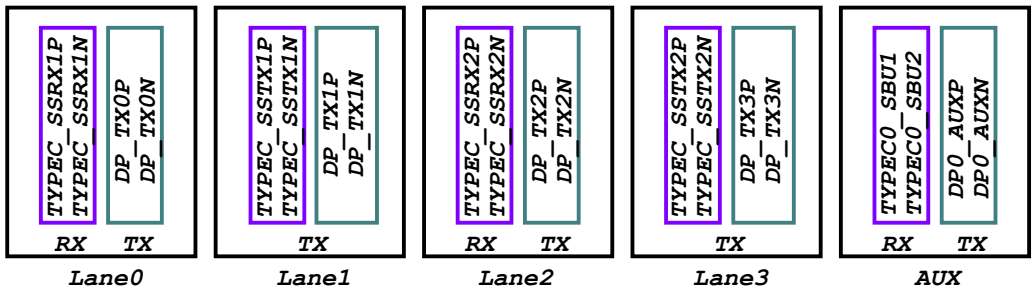
HINLINK		
Project:	H88K_V3.1	HINLINK
File:	06.Lower-Speed Bus Map	
Date:	Monday, May 06, 2024	Rev: <Revision>
Designer:	<designer>	Sheet: 6 of 43

USB Controller Configure Table

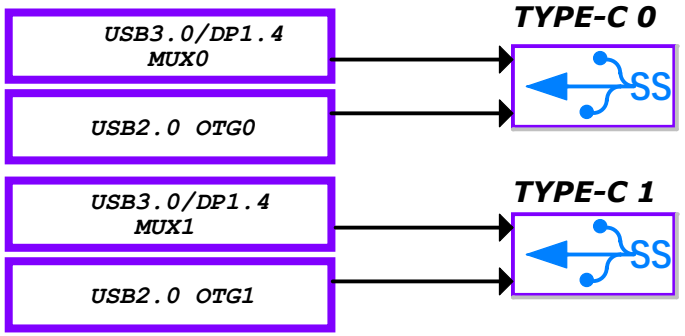
Controller Name	Pin Name	Type-C Function	DPx4Lane Function		USB30 HOST+DPx2Lane Function		USB20 HOST+DPx2Lane Function		USB20 HOST+DPx4Lane Function	
			OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2
USB30 OTG0 Device or Host	TYPEC0_SBU1/DP0_AUXP TYPEC0_SBU2/DP0_AUXN	TYPEC0_SBU1 TYPEC0_SBU2	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN
	TYPEC0_SSRX1P/DP0_TX0P TYPEC0_SSRX1N/DP0_TX0N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX0P DP0_TX0N		DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N
	TYPEC0_SSTX1P/DP0_TX1P TYPEC0_SSTX1N/DP0_TX1N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX1P DP0_TX1N		DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N
	TYPEC0_SSRX2P/DP0_TX2P TYPEC0_SSRX2N/DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N		DP0_TX2P DP0_TX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N
	TYPEC0_SSTX2P/DP0_TX3P TYPEC0_SSTX2N/DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N		DP0_TX3P DP0_TX3N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N
USB20 OTG0 Device or Host	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM			TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM
USB30 OTG1 Device or Host	TYPEC1_SBU1/DP1_AUXP TYPEC1_SBU2/DP1_AUXN	TYPEC1_SBU1 TYPEC1_SBU2	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN
	TYPEC1_SSRX1P/DP1_TX0P TYPEC1_SSRX1N/DP1_TX0N	TYPEC1_SSRX1P TYPEC1_SSRX1N	DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N	TYPEC1_SSRX1P TYPEC1_SSRX1N	DP1_TX0P DP1_TX0N	DP1_TX0P DP1_TX0N		DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N
	TYPEC1_SSTX1P/DP1_TX1P TYPEC1_SSTX1N/DP1_TX1N	TYPEC1_SSTX1P TYPEC1_SSTX1N	DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N	TYPEC1_SSTX1P TYPEC1_SSTX1N	DP1_TX1P DP1_TX1N	DP1_TX1P DP1_TX1N		DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N
	TYPEC1_SSRX2P/DP1_TX2P TYPEC1_SSRX2N/DP1_TX2N	TYPEC1_SSRX2P TYPEC1_SSRX2N	DP1_TX2P DP1_TX2N	DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N	TYPEC1_SSRX2P TYPEC1_SSRX2N		DP1_TX2P DP1_TX2N	DP1_TX2P DP1_TX2N	DP1_TX0P DP1_TX0N
	TYPEC1_SSTX2P/DP1_TX3P TYPEC1_SSTX2N/DP1_TX3N	TYPEC1_SSTX2P TYPEC1_SSTX2N	DP1_TX3P DP1_TX3N	DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N	TYPEC1_SSTX2P TYPEC1_SSTX2N		DP1_TX3P DP1_TX3N	DP1_TX3P DP1_TX3N	DP0_TX1P DP0_TX1N
USB20 OTG1 Device or Host	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM			TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM
			OPTION1 USB30 HOST		OPTION2 USB30 HOST	USB30 OTG or Device				
USB30 OTG2 Device or Host	PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN		USB30_2_SSTXP USB30_2_SSTXN		USB30_2_SSTXP USB30_2_SSTXN	USB30_2_SSTXP USB30_2_SSTXN				
	PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN		USB30_2_SSRXP USB30_2_SSRXN		USB30_2_SSRXP USB30_2_SSRXN	USB30_2_SSRXP USB30_2_SSRXN				
USB20 HOST0	USB20_HOST0_DP USB20_HOST0_DM		USB20_HOST0_DP USB20_HOST0_DM							
USB20 HOST1	USB20_HOST1_DP USB20_HOST1_DM				USB20_HOST1_DP USB20_HOST1_DM					
						TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM				

Note:
DP Lane swap enable
0:Lane0/1/2/3 TxData mapping to Lane0/1/2/3_TXDP/N
1:Lane0/1/2/3 TxData mapping to Lane2/3/0/1_TXDP/N

USB3.0/DP1.4 Lane Diagram

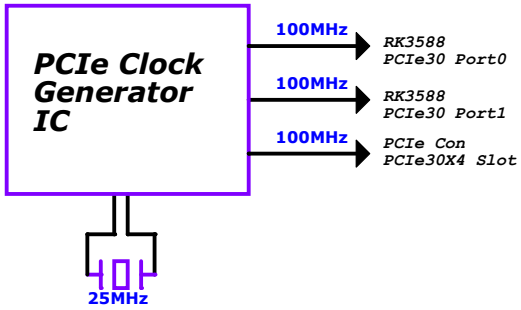


TYPE-C Connector Diagram

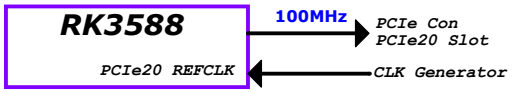


HINLINK			
Project:	H88K_V3.1		
File:	07.USB Controller Configure Tab		
Date:	Monday, May 06, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	7 of 43

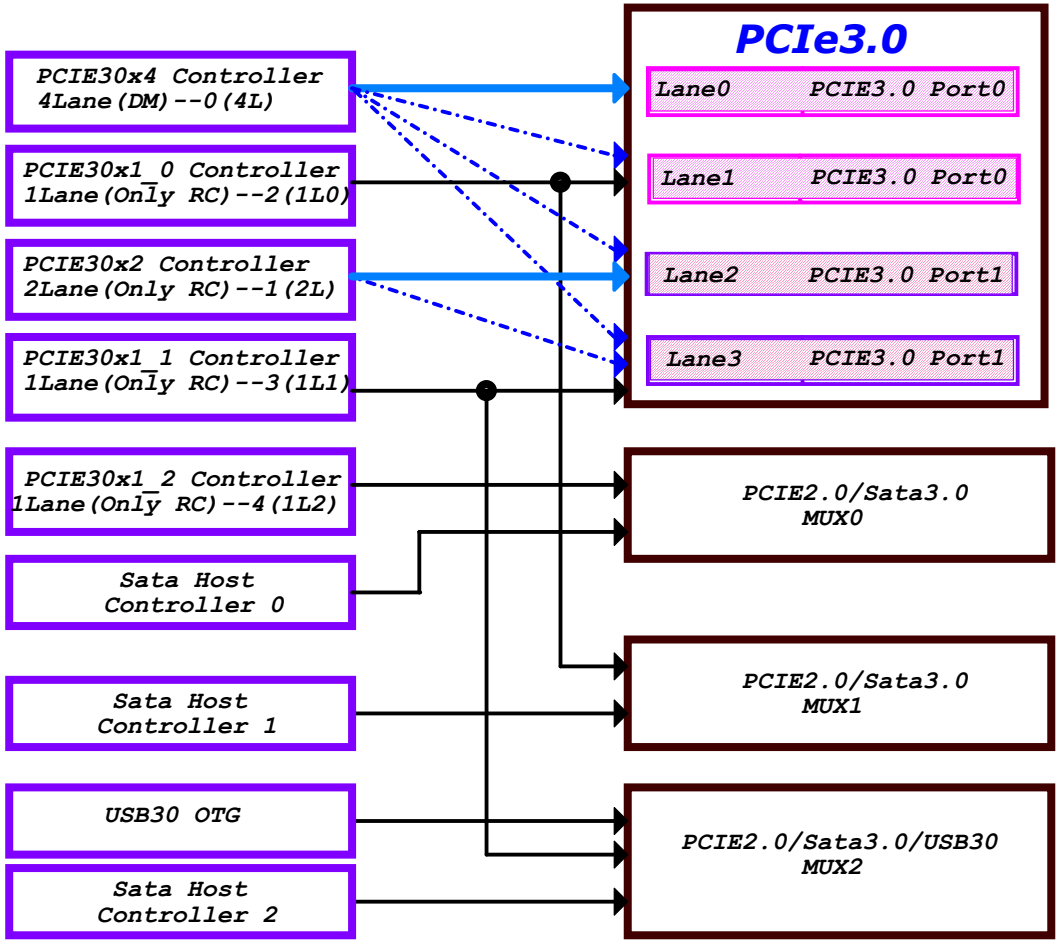
PCIe3.0 REFCLK



PCIe2.0 REFCLK



PCIe/SATA Connecter Diagram



PCIe Controller Configure Table

Controller Name	Data & Clk Lane Configure			Control GPIO
	OPTION	CLK LANE	DATA LANE	
PCIE30X4 RC & EP	OPTION1	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0	PCIE30X4_CLKREQ_M* PCIE30X4_WAKEN_M* PCIE30X4_PERSTN_M* PCIE30X4_BUTTON_RSTN
	OPTION2	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0 PCIE30_PORT0_TX1 PCIE30_PORT0_RX1	
	OPTION3	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT1_TX0 PCIE30_PORT0_RX0 PCIE30_PORT1_RX0 PCIE30_PORT0_TX1 PCIE30_PORT1_TX1 PCIE30_PORT0_RX1 PCIE30_PORT1_RX1	
PCIE30X2 RC	OPTION1	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX0 PCIE30_PORT1_RX0	PCIE30X2_CLKREQ_M* PCIE30X2_WAKEN_M* PCIE30X2_PERSTN_M* PCIE30X2_BUTTON_RSTN
	OPTION2	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX0 PCIE30_PORT1_RX0 PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	
PCIE30X1_0 RC	OPTION1	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX1 PCIE30_PORT0_RX1	PCIE30X1_0_CLKREQ_M* PCIE30X1_0_WAKEN_M* PCIE30X1_0_PERSTN_M* PCIE30X1_0_BUTTON_RSTN
	OPTION2	PCIE20_1_REFCLKP PCIE20_1_REFCLKN	PCIE20_1_TXP PCIE20_1_RXP PCIE20_1_TXN PCIE20_1_RXN	
PCIE30X1_1 RC	OPTION1	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	PCIE30X1_1_CLKREQ_M* PCIE30X1_1_WAKEN_M* PCIE30X1_1_PERSTN_M* PCIE30X1_1_BUTTON_RSTN
	OPTION2	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TXP PCIE20_2_RXP PCIE20_2_TXN PCIE20_2_RXN	
PCIE30X1_2 RC	OPTION1	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TXP PCIE20_0_RXP PCIE20_0_TXN PCIE20_0_RXN	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

Note:
PCIE30_PORT*_REF_CLKP/N is input gpio

PCIE20_*_REFCLKP/N is output or input gpio

Note:
M*=Mean to M0 or M1,It's the same source,Just multiplex to M0 or M1, So,Only use one at the same time.

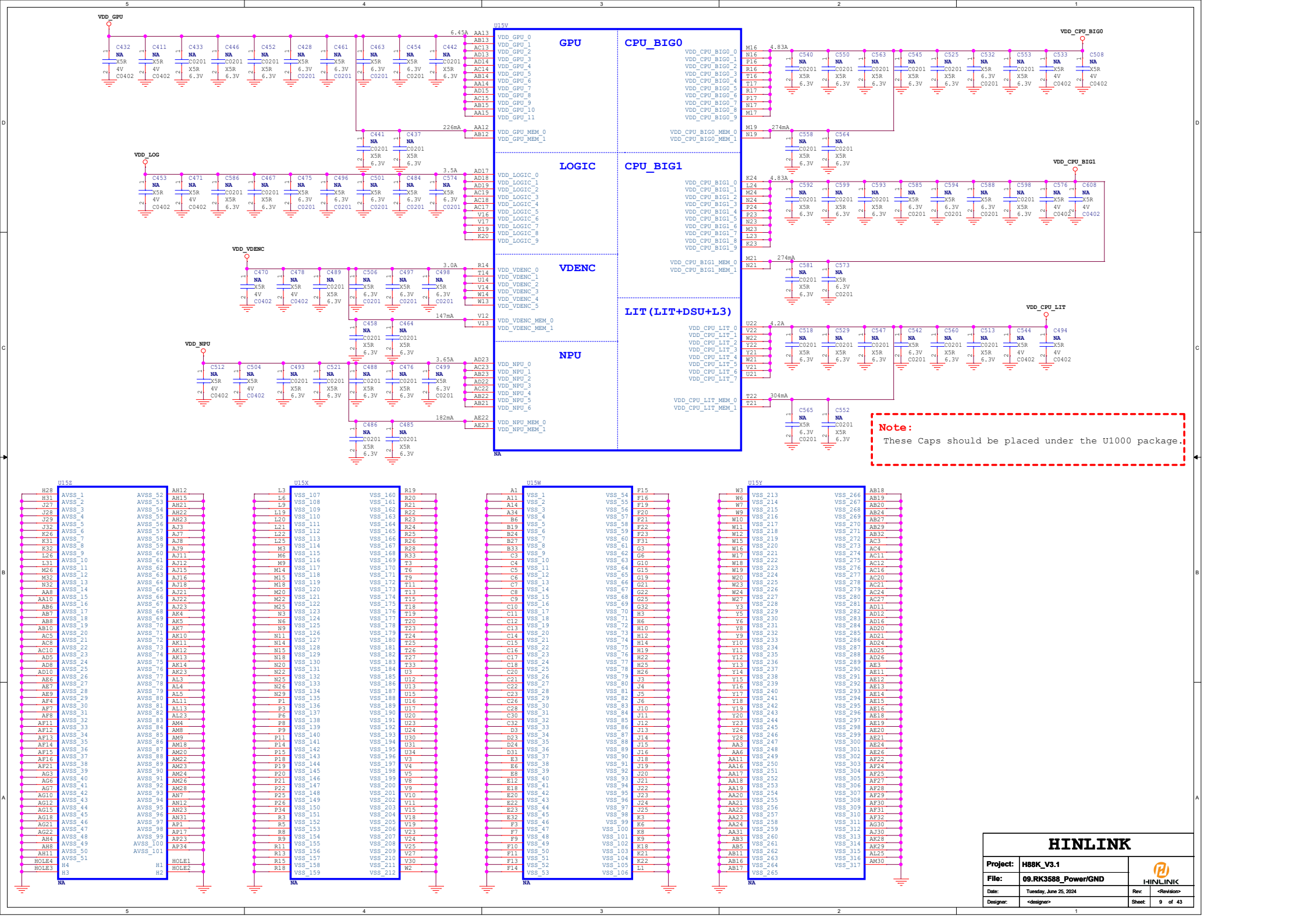
PCIe/SATA Function Combination

Function Combination

Function Item	PCIEX4	PCIEX2	PCIEX1	SATA
Option1	1(DM)	0	3(RC)	0
Option2	1(DM)	0	2(RC)	1
Option3	1(DM)	0	1(RC)	2
Option4	1(DM)	0	0	3
Option5	0	1(DM)+1(RC)	3(RC)	0
Option6	0	1(DM)+1(RC)	2(RC)	1
Option7	0	1(DM)+1(RC)	1(RC)	2
Option8	0	1(DM)+1(RC)	0	3
Option9	0	1(DM)	4(RC)	1
Option10	0	1(DM)	3(RC)	2
Option11	0	1(DM)	2(RC)	3
Option12	0	0	5(RC)	2
Option13	0	0	4(RC)	3

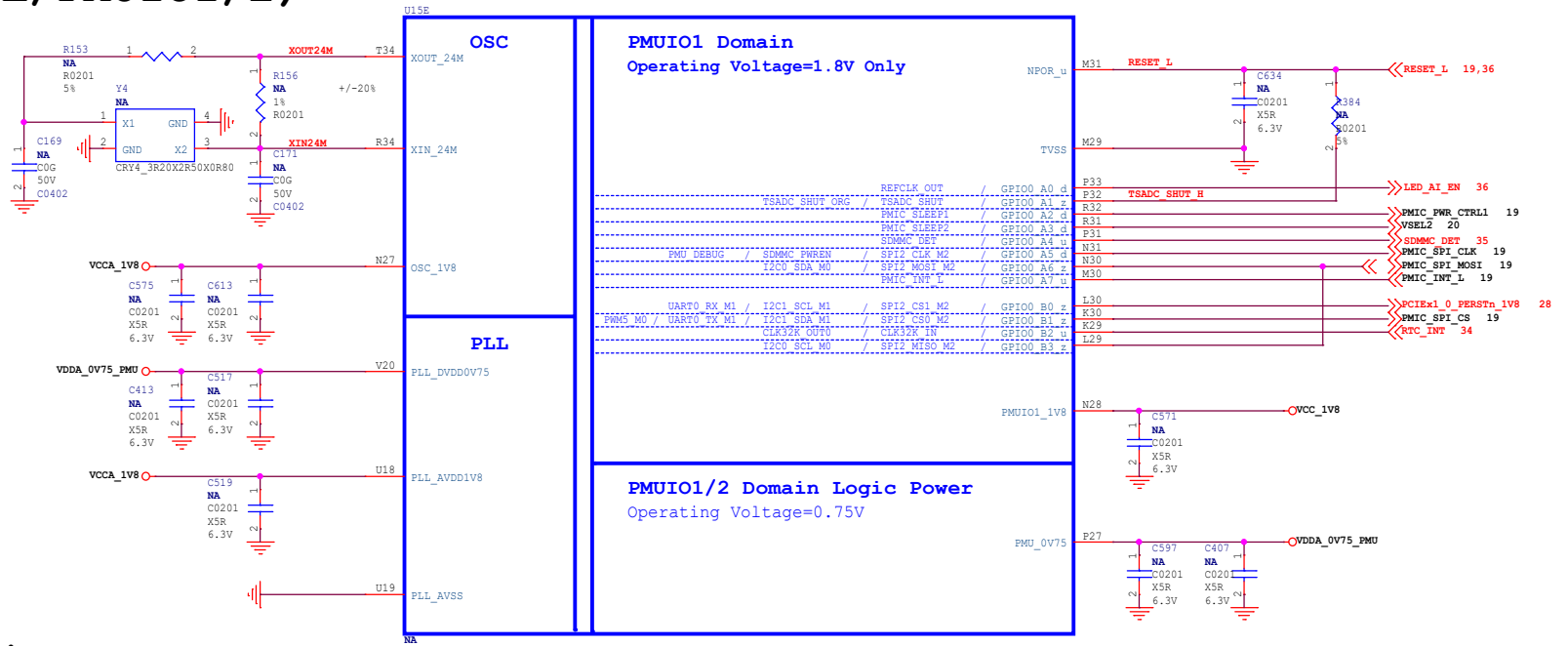
HINLINK

Project:	H88K_V3.1		
File:	08.PCIE Fun Map		
Date:	Monday, May 06, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	8 of 43

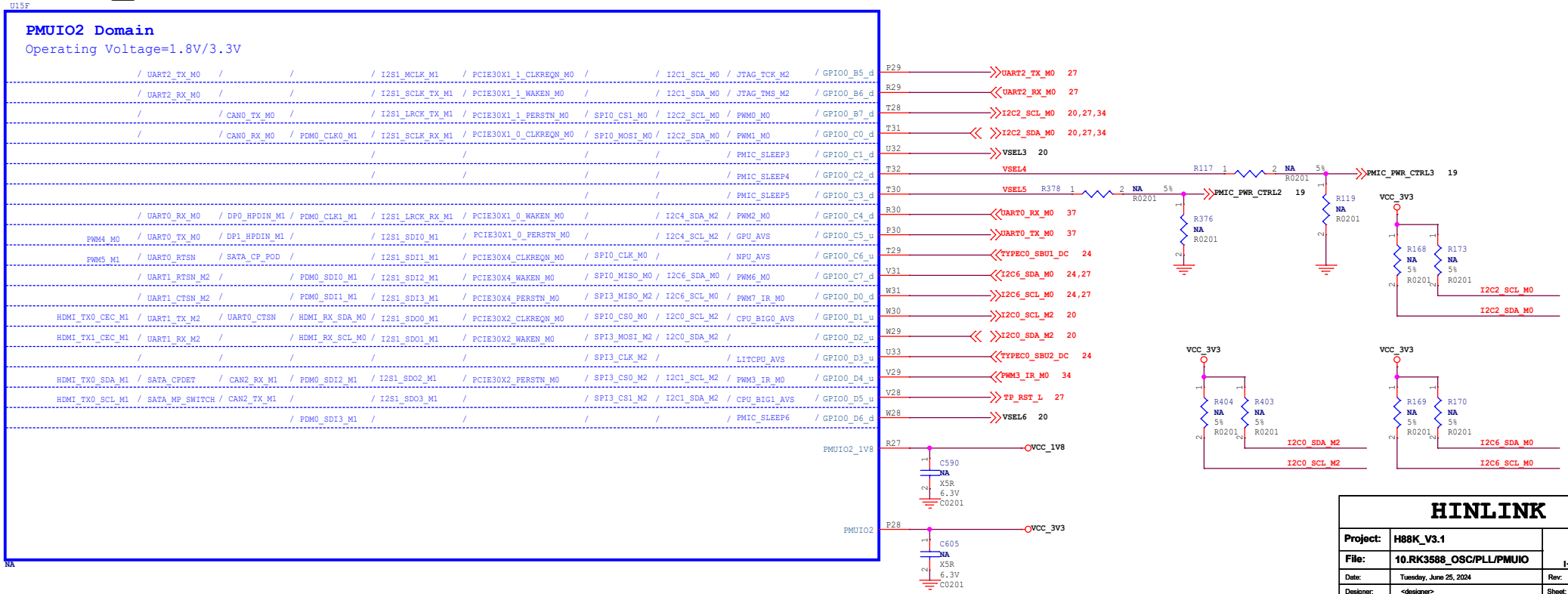


HINLINK			
Project:	H88K_V3.1		
File:	09.RK3588_Power/GND		
Date:	Tuesday, June 25, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	9 of 43

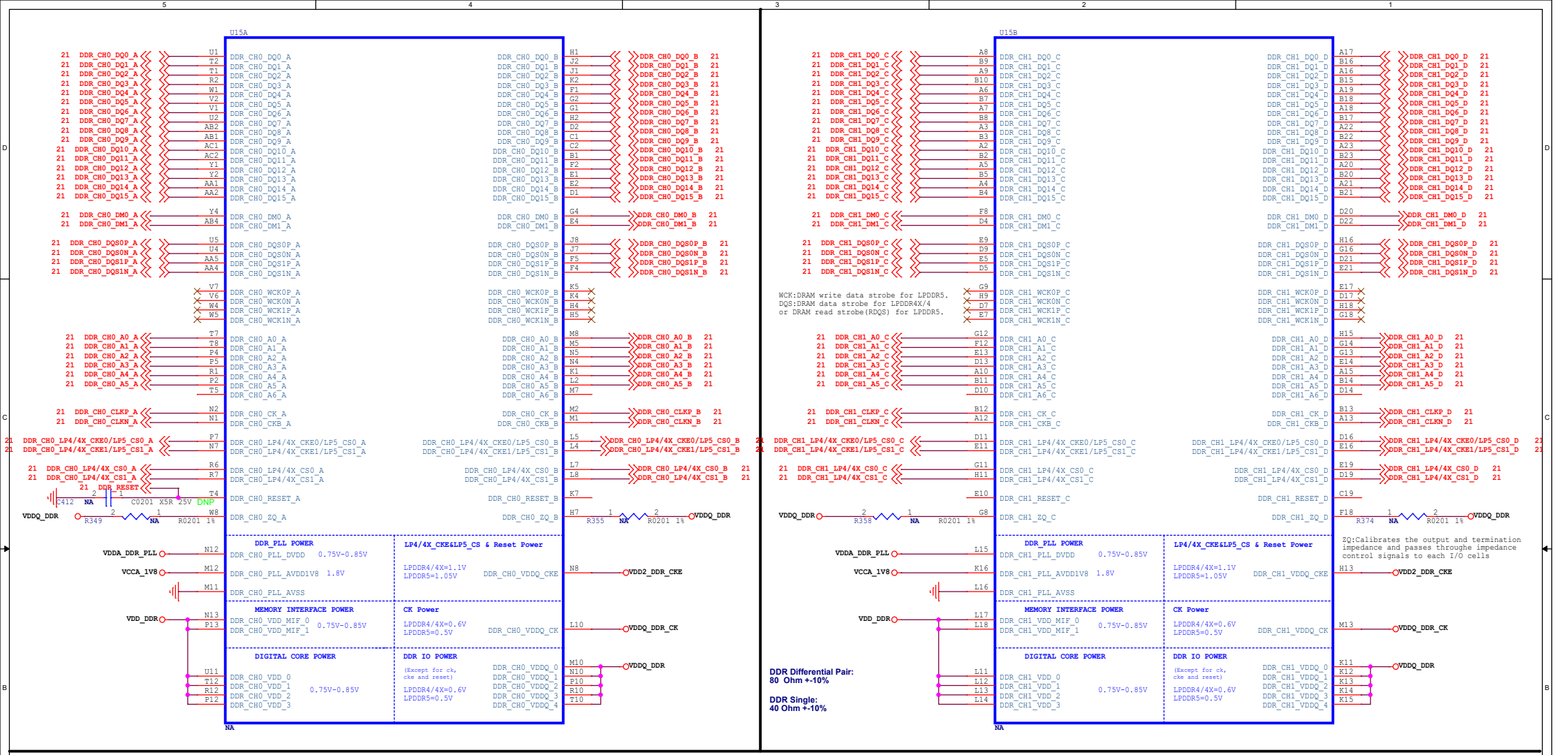
RK3588_E(OSC/PLL/PMUIO1/2)



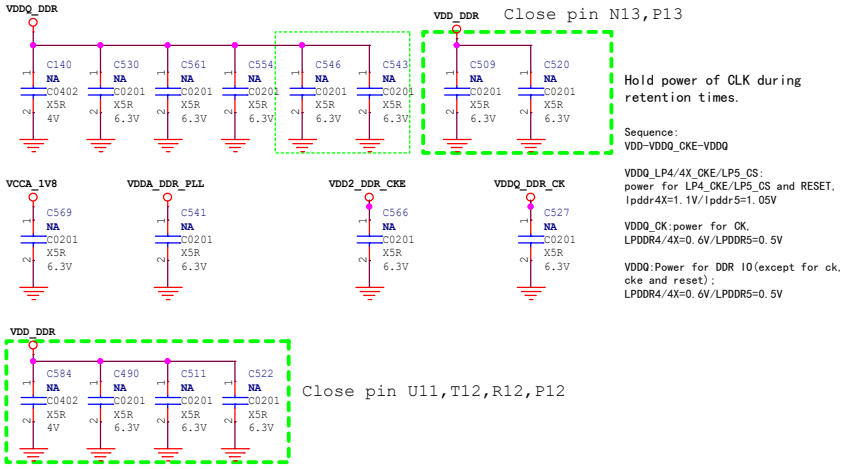
RK3588_F(PMUIO2)



HINLINK			
Project:	H88K_V3.1		
File:	10.RK3588_OSC/PLL/PMUIO		
Date:	Tuesday, June 25, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	10 of 43



DDR FILTER



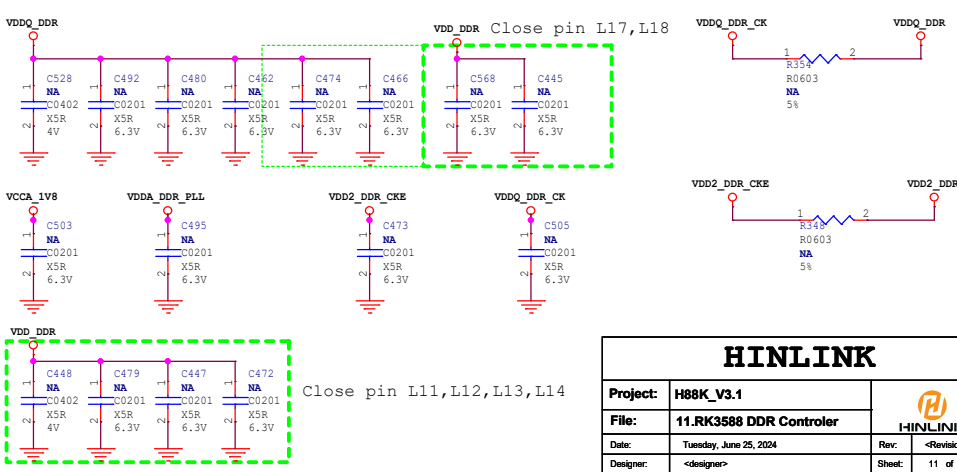
Hold power of CLK during retention times.

Sequence:
VDD-VDDQ_CKE-VDDQ

VDDQ_LP4/4X_CKE/LP5_CS:
power for LP4_CKE/LP5_CS and RESET.
Ipddr4X=1.1V/Ipddr5=1.05V

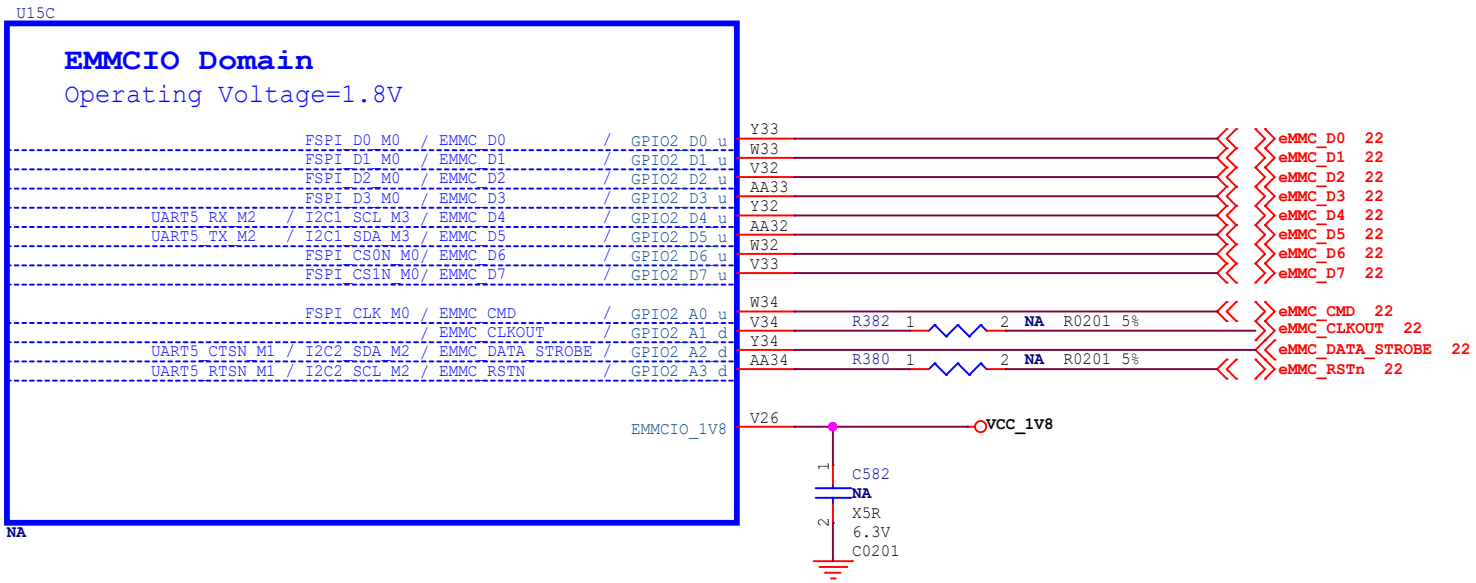
VDDQ_CK:power for CK.
LPDDR4/4X=0.6V/LPDDR5=0.5V

VDDQ:Power for DDR IO(except for ck, cke and reset);
LPDDR4/4X=0.6V/LPDDR5=0.5V

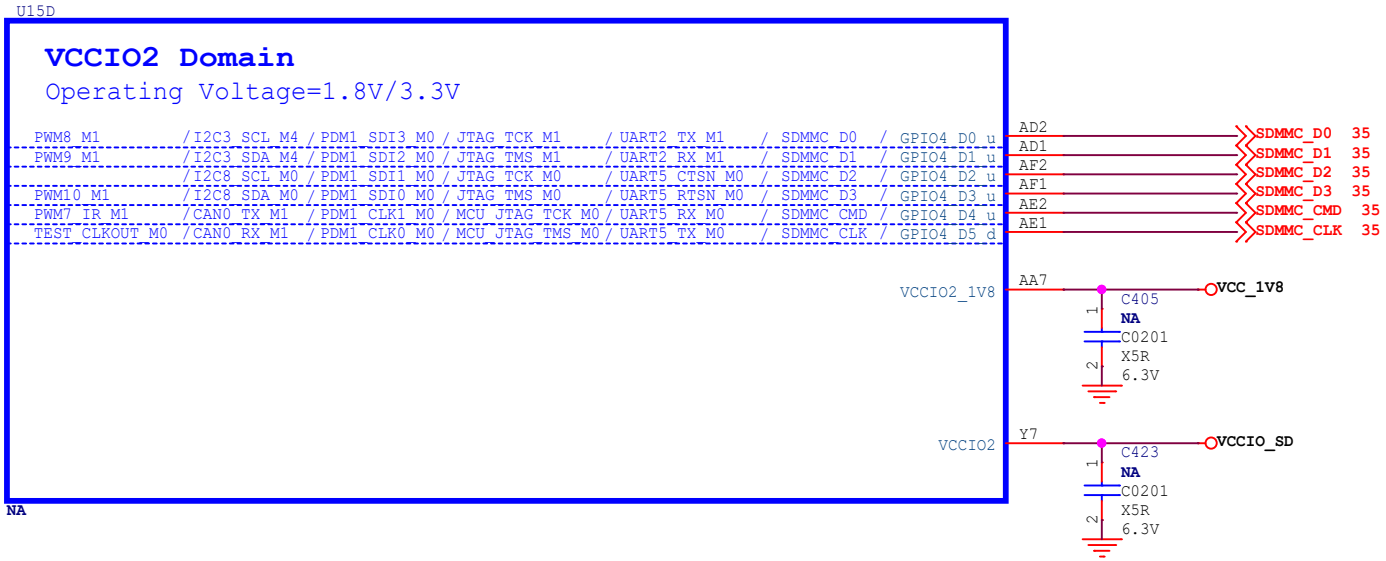


HINLINK			
Project:	H88K_V3.1		
File:	11.RK3588 DDR Controler		
Date:	Tuesday, June 25, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	11 of 43

RK3588_C(EMMCIO Domain)

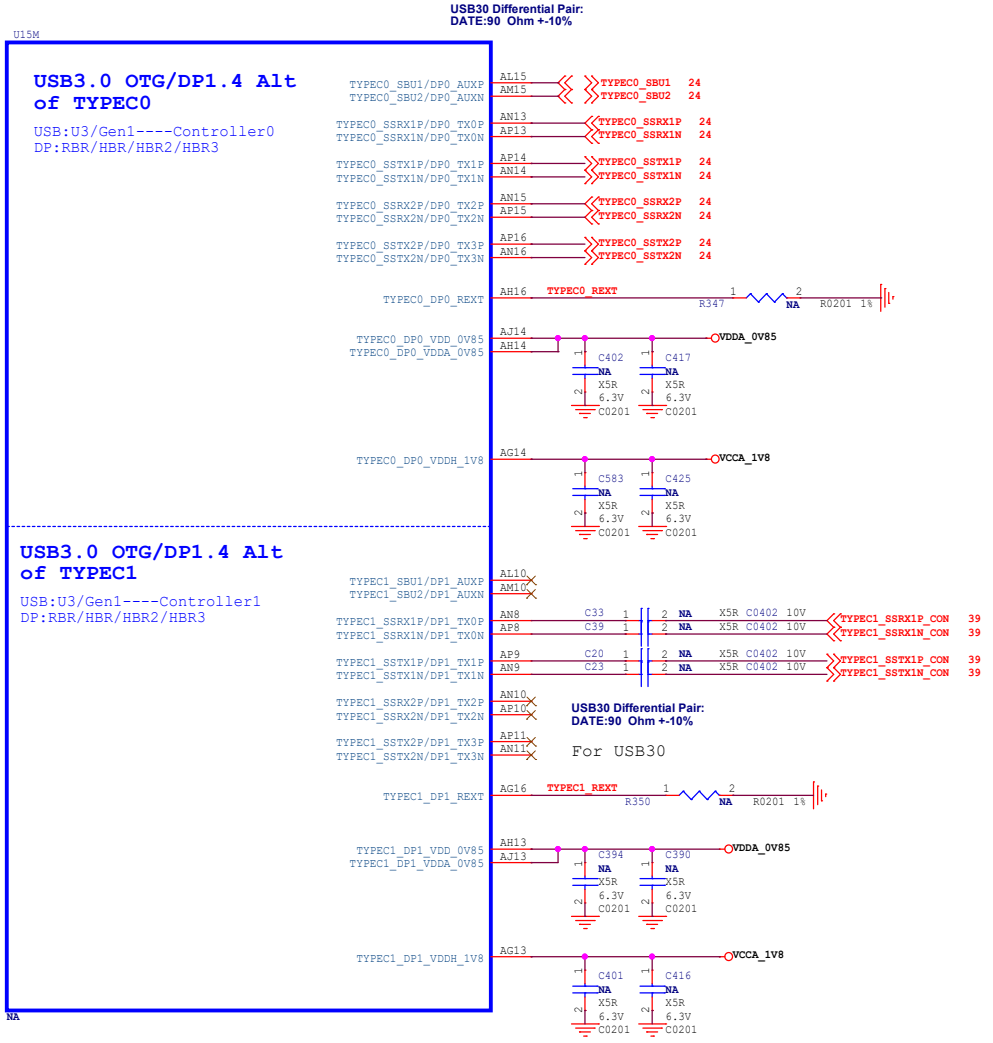


RK3588_D(VCCIO2 Domain)



HINLINK			
Project:	H88K_V3.1		
File:	12.RK3588_Flash/SD Controller		
Date:	Tuesday, June 25, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	12 of 43

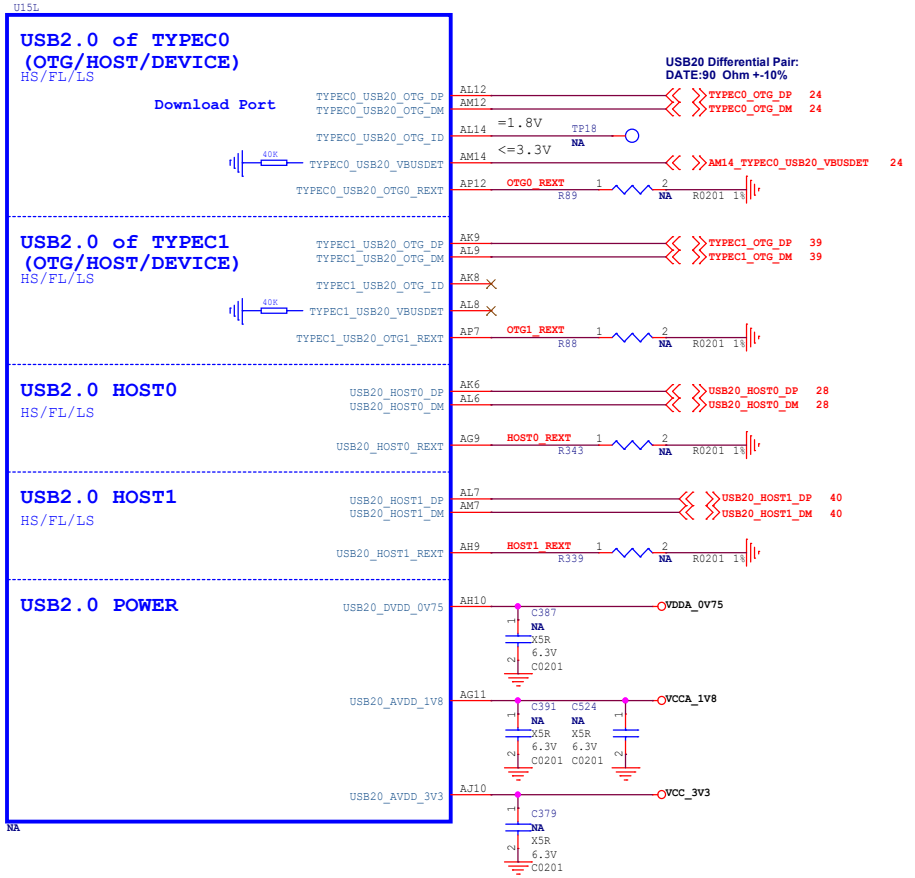
RK3588_M(TYPEC/DP)



USB30/DP1.4 Alt Mode Configuration

Option1	*DP x4Lane*	*DP_TX_Lane0-3*
Option2	*USB30 x4Lane*	*DP_TX_Lane0-3*
Option3	*USB30X2Lane+DPX2Lane*	*USB30:Lane0 Lane1* *DP:Lane2 Lane3*
Option4	*USB30X2Lane+DPX2Lane*	*USB30:Lane2 Lane3* *DP:Lane0 Lane1*

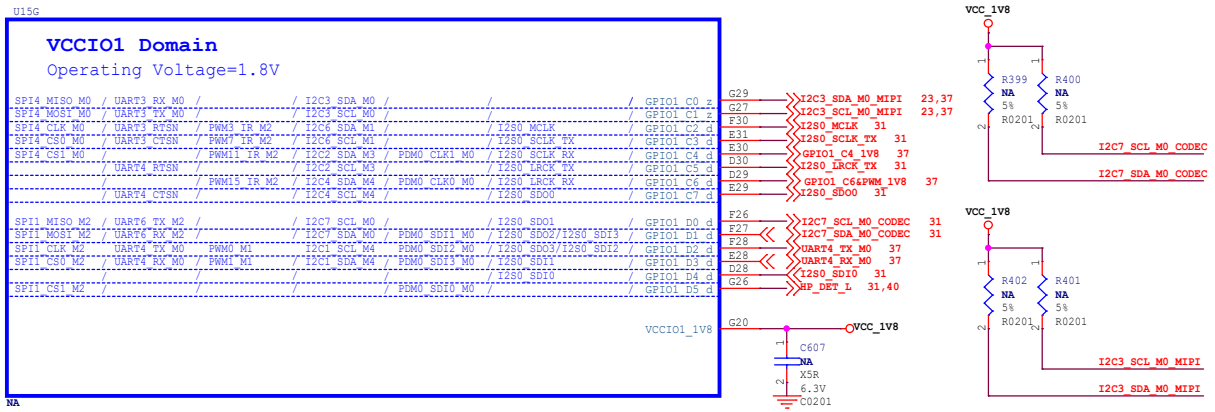
RK3588_L(USB2.0 HOST/OTG)



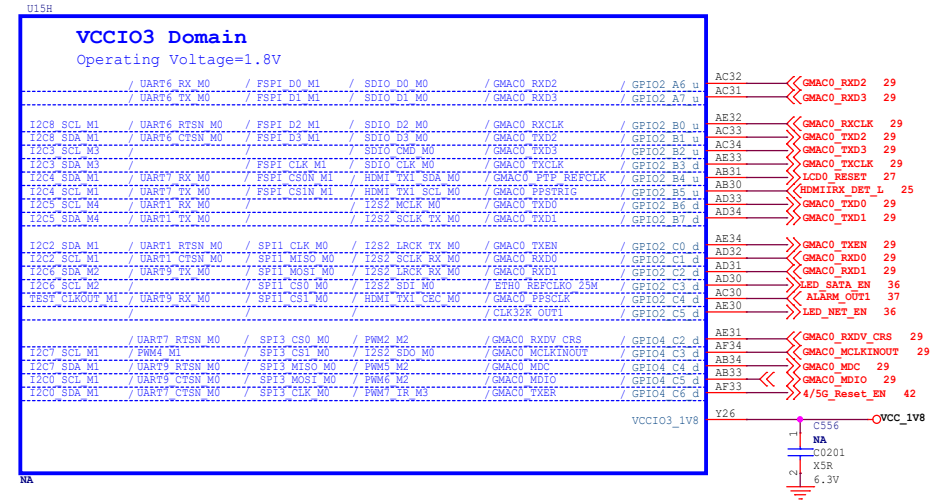
Note:
The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 30K ohm resistor.The VBUSDETpin voltage range <=3.3V.

HINLINK		
Project:	H88K_V3.1	HINLINK
File:	13.RK3588_USB30/USB20_Ctrl	
Date:	Tuesday, June 25, 2024	Rev: <Revision>
Designer:	<designer>	Sheet: 13 of 43

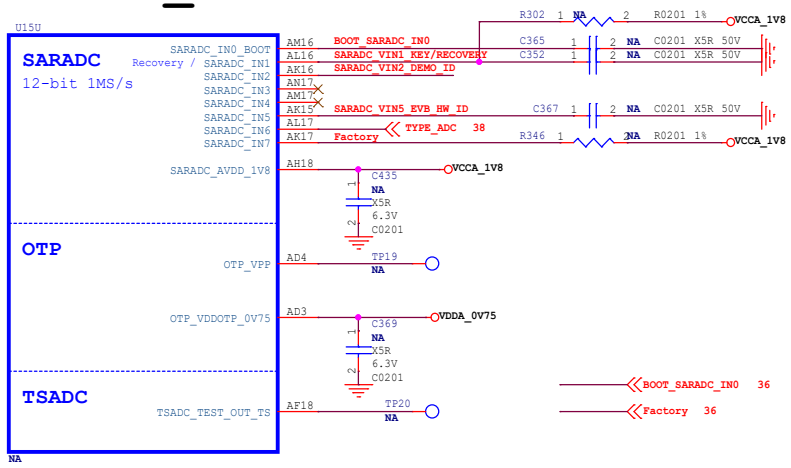
RK3588_G(VCCIO1 Domain)



RK3588_H(VCCIO3 Domain)



RK3588_U(SARADC/OTP)



BOOT MODE CONFIG

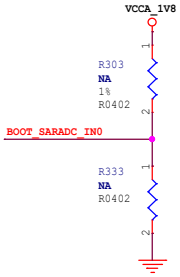


TABLE 1

Item	Rup	Rdown	ADC	VOL	BOOT MODE
LEVEL1	DNP	100K	0	0V	USB
LEVEL2	100K	20K	682	0.3V	SD Card-USB
LEVEL3	360K	180K	1365	0.6V	EMMC-USB
LEVEL4	100K	100K	2047	0.9V	FSPI M0-USB
LEVEL5	180K	360K	2730	1.2V	FSPI M1-USB
LEVEL6	20K	100K	3412	1.5V	FSPI M2-USB
LEVEL7	100K	DNP	4095	1.8V	FSPI_M2-FSPI_M1-FSPI_M0 -EMMC-SD Card-USB

BOARD_ID CONFIG

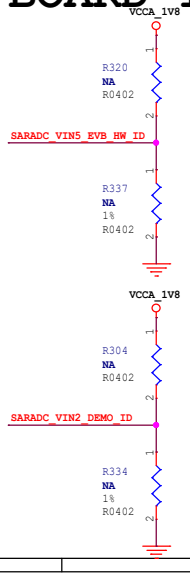


TABLE 2

Item	Rup	Rdown	ADC	VOL	VERSION
LEVEL1	DNP	100K	0	0V	V1.0
LEVEL2	100K	20K	682	0.3V	V2.0
LEVEL3	360K	180K	1365	0.6V	V3.0
LEVEL4	100K	100K	2047	0.9V	V4.0
LEVEL5	180K	360K	2730	1.2V	V5.0
LEVEL6	20K	100K	3412	1.5V	V6.0
LEVEL7	100K	DNP	4095	1.8V	V7.0

HINLINK			
Project:	H88K_V3.1		
File:	14.RK3588_SARADC/1.8V Only GPIO		
Date:	Tuesday, June 25, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	14 of 43

RK3588_Q/R(MIPI_D/C_PHY0/1)

U15Q

MIPI D/C-PHY DSI_TX Port0

D-PHY:V1.2 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY0_TX_CLKP/MIPI_CPHY0_TX_TRIO1_C — AN26 — MIPI_DPHY0_TX_CLKP 27
MIPI_DPHY0_TX_CLKN/MIPI_CPHY0_TX_TRIO1_B — AP26 — MIPI_DPHY0_TX_CLKN 27
MIPI_DPHY0_TX_D0P/MIPI_CPHY0_TX_TRIO0_B — AN24 — MIPI_DPHY0_TX_D0P 27
MIPI_DPHY0_TX_D0N/MIPI_CPHY0_TX_TRIO0_A — AP24 — MIPI_DPHY0_TX_D0N 27
MIPI_DPHY0_TX_D1P/MIPI_CPHY0_TX_TRIO1_A — AN25 — MIPI_DPHY0_TX_D1P 27
MIPI_DPHY0_TX_D1N/MIPI_CPHY0_TX_TRIO0_C — AP25 — MIPI_DPHY0_TX_D1N 27
MIPI_DPHY0_TX_D2P/MIPI_CPHY0_TX_TRIO2_B — AN27 — MIPI_DPHY0_TX_D2P 27
MIPI_DPHY0_TX_D2N/MIPI_CPHY0_TX_TRIO2_A — AP27 — MIPI_DPHY0_TX_D2N 27
MIPI_DPHY0_TX_D3P/NO_USE — AN28 — MIPI_DPHY0_TX_D3P 27
MIPI_DPHY0_TX_D3N/MIPI_CPHY0_TX_TRIO2_C — AP28 — MIPI_DPHY0_TX_D3N 27

MIPI D/C-PHY CSI_RX Port0

D-PHY:V1.2 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY0_RX_CLKP/MIPI_CPHY0_RX_TRIO1_C — AN32 — MIPI_DPHY0_RX_CLKP 23
MIPI_DPHY0_RX_CLKN/MIPI_CPHY0_RX_TRIO1_B — AP31 — MIPI_DPHY0_RX_CLKN 23
MIPI_DPHY0_RX_D0P/MIPI_CPHY0_RX_TRIO0_B — AN29 — MIPI_DPHY0_RX_D0P 23
MIPI_DPHY0_RX_D0N/MIPI_CPHY0_RX_TRIO0_A — AP29 — MIPI_DPHY0_RX_D0N 23
MIPI_DPHY0_RX_D1P/MIPI_CPHY0_RX_TRIO1_A — AN30 — MIPI_DPHY0_RX_D1P 23
MIPI_DPHY0_RX_D1N/MIPI_CPHY0_RX_TRIO0_C — AP30 — MIPI_DPHY0_RX_D1N 23
MIPI_DPHY0_RX_D2P/MIPI_CPHY0_RX_TRIO2_B — AN33 — MIPI_DPHY0_RX_D2P 23
MIPI_DPHY0_RX_D2N/MIPI_CPHY0_RX_TRIO2_A — AP32 — MIPI_DPHY0_RX_D2N 23
MIPI_DPHY0_RX_D3P/NO_USE — AN34 — MIPI_DPHY0_RX_D3P 23
MIPI_DPHY0_RX_D3N/MIPI_CPHY0_RX_TRIO2_C — AP33 — MIPI_DPHY0_RX_D3N 23

MIPI D/C-PHY POWER

MIPI_D/C_PHY0_VREG — AF20 — C468 NA — 2 C0201 X7R 6.3V
MIPI_D/C_PHY0_VDD — AG20 — VDDA_0V75
C459 NA X5R 6.3V C0201; C548 NA X5R 6.3V C0201
D-PHY 4.5Gbps & C-PHY 2.5Gsps 0.85V
D-PHY 2.5Gbps & C-PHY 1.5Gsps 0.75V
MIPI_D/C_PHY0_VDD_1V2 — AH20 — VCCA1V2_IMAGE
C449 NA X5R 6.3V C0201; C414 NA X5R 6.3V C0201
MIPI_D/C_PHY0_VDD_1V8 — AJ20 — VCCA1V8_IMAGE
C443 NA X5R 6.3V C0201; C397 NA X5R 6.3V C0201

NA

U15R

MIPI D/C-PHY DSI_TX Port1

D-PHY:V1.2 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY1_TX_CLKP/MIPI_CPHY1_TX_TRIO1_C — AN20 — MIPI_DPHY1_TX_CLKP 27
MIPI_DPHY1_TX_CLKN/MIPI_CPHY1_TX_TRIO1_B — AP20 — MIPI_DPHY1_TX_CLKN 27
MIPI_DPHY1_TX_D0P/MIPI_CPHY1_TX_TRIO0_B — AN18 — MIPI_DPHY1_TX_D0P 27
MIPI_DPHY1_TX_D0N/MIPI_CPHY1_TX_TRIO0_A — AP18 — MIPI_DPHY1_TX_D0N 27
MIPI_DPHY1_TX_D1P/MIPI_CPHY1_TX_TRIO1_A — AN19 — MIPI_DPHY1_TX_D1P 27
MIPI_DPHY1_TX_D1N/MIPI_CPHY1_TX_TRIO0_C — AP19 — MIPI_DPHY1_TX_D1N 27
MIPI_DPHY1_TX_D2P/MIPI_CPHY1_TX_TRIO2_B — AN21 — MIPI_DPHY1_TX_D2P 27
MIPI_DPHY1_TX_D2N/MIPI_CPHY1_TX_TRIO2_A — AP21 — MIPI_DPHY1_TX_D2N 27
MIPI_DPHY1_TX_D3P/NO_USE — AN22 — MIPI_DPHY1_TX_D3P 27
MIPI_DPHY1_TX_D3N/MIPI_CPHY1_TX_TRIO2_C — AP22 — MIPI_DPHY1_TX_D3N 27

MIPI D/C-PHY CSI_RX Port1

D-PHY:V1.2 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY1_RX_CLKP/MIPI_CPHY1_RX_TRIO1_C — AK20 — MIPI_DPHY1_RX_CLKP 23
MIPI_DPHY1_RX_CLKN/MIPI_CPHY1_RX_TRIO1_B — AL20 — MIPI_DPHY1_RX_CLKN 23
MIPI_DPHY1_RX_D0P/MIPI_CPHY1_RX_TRIO0_B — AK18 — MIPI_DPHY1_RX_D0P 23
MIPI_DPHY1_RX_D0N/MIPI_CPHY1_RX_TRIO0_A — AL18 — MIPI_DPHY1_RX_D0N 23
MIPI_DPHY1_RX_D1P/MIPI_CPHY1_RX_TRIO1_A — AK19 — MIPI_DPHY1_RX_D1P 23
MIPI_DPHY1_RX_D1N/MIPI_CPHY1_RX_TRIO0_C — AL19 — MIPI_DPHY1_RX_D1N 23
MIPI_DPHY1_RX_D2P/MIPI_CPHY1_RX_TRIO2_B — AK21 — MIPI_DPHY1_RX_D2P 23
MIPI_DPHY1_RX_D2N/MIPI_CPHY1_RX_TRIO2_A — AL21 — MIPI_DPHY1_RX_D2N 23
MIPI_DPHY1_RX_D3P/NO_USE — AK22 — MIPI_DPHY1_RX_D3P 23
MIPI_DPHY1_RX_D3N/MIPI_CPHY1_RX_TRIO2_C — AL22 — MIPI_DPHY1_RX_D3N 23

MIPI D/C-PHY POWER

MIPI_D/C_PHY1_VREG — AF19 — C451 NA — 2 C0201 X7R 6.3V
MIPI_D/C_PHY1_VDD — AG19 — VDDA_0V75
C444 NA X5R 6.3V C0201
MIPI_D/C_PHY1_VDD_1V2 — AH19 — VCCA1V2_IMAGE
C440 NA X5R 6.3V C0201
MIPI_D/C_PHY1_VDD_1V8 — AJ19 — VCCA1V8_IMAGE
C436 NA X5R 6.3V C0201

NA

Note:
These Caps should be placed under the U1000 package.

RK3588_P(MIPI_CSI_RX_PHY)

U15P

MIPI DPHY CSI_RX Port0

MIPI V1.2/2.5Gbps

MIPI_CSI0_CLK0P/MIPI_CSI0_CLK0N — AJ33/AJ34 — MIPI_CSI0_RX_CLK0P/MIPI_CSI0_RX_CLK0N 23
MIPI_CSI0_D0P/MIPI_CSI0_D0N — AG33/AG34 — MIPI_CSI0_RX_D0P/MIPI_CSI0_RX_D0N 23
MIPI_CSI0_D1P/MIPI_CSI0_D1N — AH33/AH34 — MIPI_CSI0_RX_D1P/MIPI_CSI0_RX_D1N 23
MIPI_CSI0_CLK1P/MIPI_CSI0_CLK1N — AM33/AM34 — MIPI_CSI0_RX_CLK1P/MIPI_CSI0_RX_CLK1N 23
MIPI_CSI0_D2P/MIPI_CSI0_D2N — AK33/AK34 — MIPI_CSI0_RX_D2P/MIPI_CSI0_RX_D2N 23
MIPI_CSI0_D3P/MIPI_CSI0_D3N — AL33/AL34 — MIPI_CSI0_RX_D3P/MIPI_CSI0_RX_D3N 23

MIPI CSI Differential Pair: 100 Ohm +-10%

MIPI_CSI0_AVCC0V75 — AB25 — VDDA_0V75
C534 NA X5R 6.3V C0201; C622 NA X5R 6.3V C0201
MIPI CSI Differential Pair: 100 Ohm +-10%
MIPI_CSI0_AVCC1V8 — AB26 — VCCA1V8_IMAGE
C408 NA X5R 6.3V C0201; C420 NA X5R 6.3V C0201

MIPI DPHY CSI_RX Port1

MIPI V1.2/2.5Gbps

MIPI_CSI1_CLK0P/MIPI_CSI1_CLK0N — AJ31/AJ32 — MIPI_CSI1_RX_CLK0P/MIPI_CSI1_RX_CLK0N 23
MIPI_CSI1_D0P/MIPI_CSI1_D0N — AG31/AG32 — MIPI_CSI1_RX_D0P/MIPI_CSI1_RX_D0N 23
MIPI_CSI1_D1P/MIPI_CSI1_D1N — AH31/AH32 — MIPI_CSI1_RX_D1P/MIPI_CSI1_RX_D1N 23
MIPI_CSI1_CLK1P/MIPI_CSI1_CLK1N — AM31/AM32 — MIPI_CSI1_RX_CLK1P/MIPI_CSI1_RX_CLK1N 23
MIPI_CSI1_D2P/MIPI_CSI1_D2N — AK31/AK32 — MIPI_CSI1_RX_D2P/MIPI_CSI1_RX_D2N 23
MIPI_CSI1_D3P/MIPI_CSI1_D3N — AL31/AL32 — MIPI_CSI1_RX_D3P/MIPI_CSI1_RX_D3N 23

MIPI_CSI1_AVCC0V75 — AA25 — VDDA_0V75
C380 NA X5R 6.3V C0201
MIPI_CSI1_AVCC1V8 — AA26 — VCCA1V8_IMAGE
C551 NA X5R 6.3V C0201

NA

Note:
Merge the two mipi csi's power need 1X105+1X104 cap.

MIPI_CSI_RX Configuration

Option1	*Sensor1 x4Lane*	*MIPI_CSI_RX_D0-3* *MIPI_CSI_RX_CLK0*
Option2	*Sensor1 x2Lane* + *Sensor2 x2Lane*	*MIPI_CSI_RX_D0-1* *MIPI_CSI_RX_CLK0*
		MIPI_CSI_RX_D2-3 *MIPI_CSI_RX_CLK1*

Note:
When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3,but clock lane1 is invalid; In dual clock lanes mode,CLK0P/0N is the clock lane of Data lane0 and Data lane1,while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

Note:
The Caps to the left of green line should be placed under the U1000 package.Other caps should be placed close to the U1000 package.

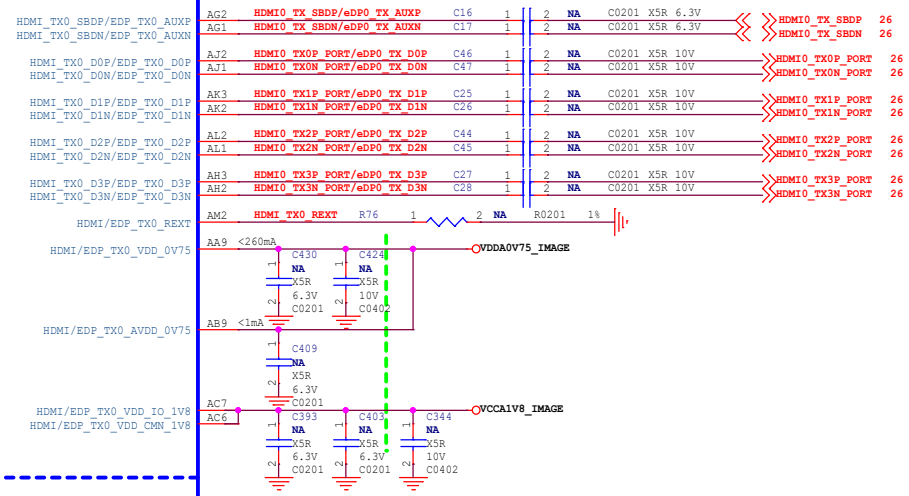
HINLINK		
Project:	H88K_V3.1	
File:	15.RK3588_MIPI Interface	HINLINK
Date:	Tuesday, June 25, 2024	Rev: <Revision>
Designer:	<designer>	Sheet: 15 of 43

RK3588_S(HDMI2.1 TX)

U15S

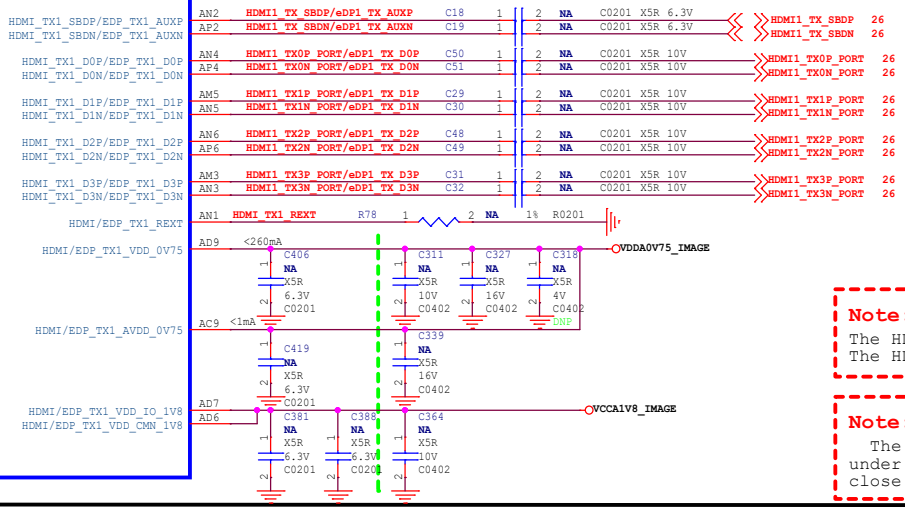
HDMI TX/eDP MUX Port0

HDMI:V2.1 12Gbps
eDP: V1.4b 5.4Gbps

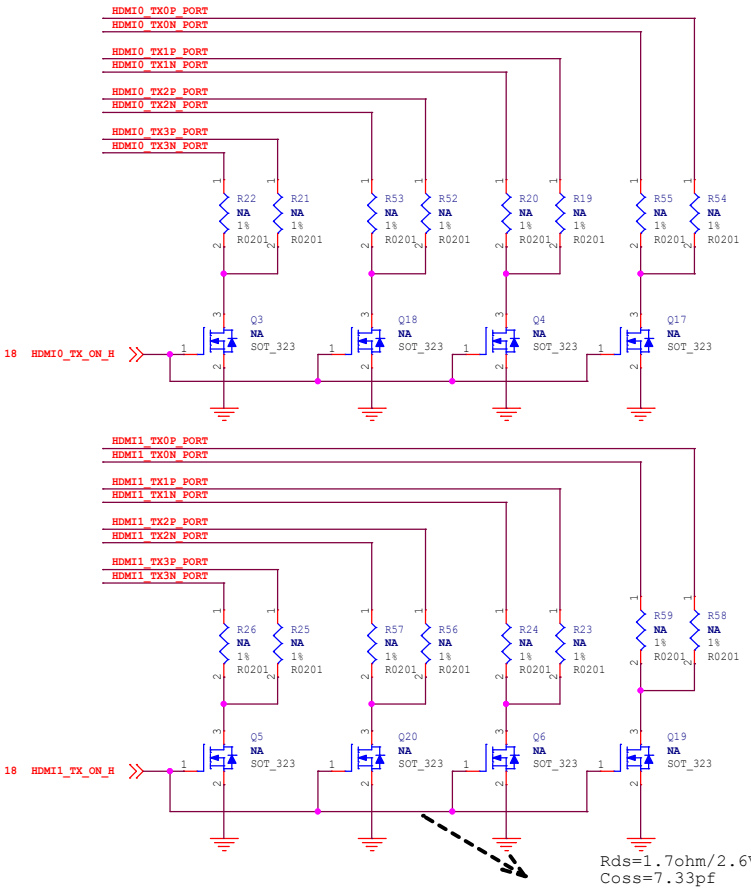


HDMI TX/eDP MUX Port1

HDMI:V2.1 12Gbps
eDP: V1.4b 5.4Gbps



NA



Note:
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.

Note:
The Caps to the left of green line should be placed under the U1000 package.Other caps should be placed close to the U1000 package.

Note:
The controller only support AC coupled link In order to backward compatibility or to meet HDMI2.0 (1.4b) DC common mode spec and Voff, need do R based level-shift.

Switch on in HDMI2.0(TMDS) mode
Switch off in HDMI2.1(FRL) mode.

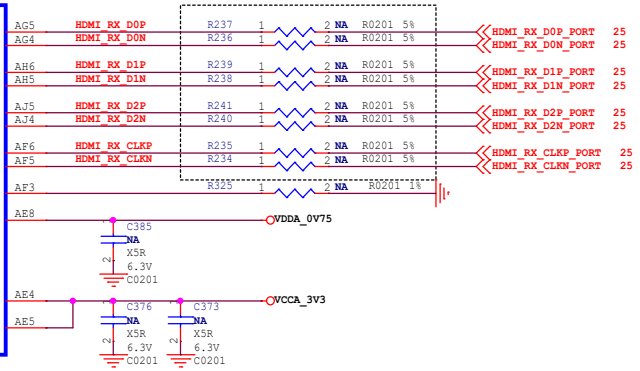
RK3588_T(HDMI20_RX)

Place close HDMI port.

U15T

HDMI RX

HDMI:V2.0



HDMI20_RX
100 Ohm +-10%

NA

HINLINK		
Project:	H88K_V3.1	
File:	16.RK3588_HDMI/eDP Interface	
Date:	Tuesday, June 25, 2024	Rev: <Revision>
Designer:	<designer>	Sheet: 16 of 43

RK3588_N(PCIE20)

CLK Differential Pair:
100 Ohm±10%
DATA Differential Pair:
PCIE20: 85 Ohm ±10%
SATA30: 100 Ohm ±10%
USB30: 90ohm ±10%

U15N

PCIE20/SATA30 Mux0

PCIe20x1_2
1Lane(RC)--4(1L2)

SATA30 HOST
Controller0

MUX

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

TO SATA PCIE 2.5G

PCIE20_0_REFCLKP
PCIE20_0_REFCLKN
L32 REFCLKP_WIFI_L32 1 — C917 — 2 NA X5R 6.3V C0201 — REFCLKP_WIFI_SATA 41
L33 REFCLKN_WIFI_L33 1 — C916 — 2 NA X5R 6.3V C0201 — REFCLKN_WIFI_SATA 41

PCIE20_0_TXP/SATA30_0_TXP
PCIE20_0_TXN/SATA30_0_TXN
M34 SATA30_TX0P C754 1 — 2 NA C0402 X5R 10V — PCIE20_0_TXP 41
M33 SATA30_TX0N C757 1 — 2 NA C0402 X5R 10V — PCIE20_0_TXN 41

PCIE20_0_RXP/SATA30_0_RXP
PCIE20_0_RXN/SATA30_0_RXN
N33 SATA30_RX0P C761 1 — 2 NA C0402 X5R 10V — PCIE20_0_RXP 41
N34 SATA30_RX0N C758 1 — 2 NA C0402 X5R 10V — PCIE20_0_RXN 41

PCIE20_SATA30_0_AVDD_0V85
M28 — C609 NA X5R 6.3V C0201 — C624 NA X5R 10V C0402 — VDDA_0V85

PCIE20_SATA30_0_AVDD_1V8
M27 — C602 NA X5R 6.3V C0201 — C659 NA X5R 10V C0402 — VCCA_1V8

PCIE20/SATA30 Mux1

PCIe30x1_0
1Lane(RC)--2(1L0)

SATA30 HOST
Controller1

MUX

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

TO WIFI

PCIE20_1_REFCLKP
PCIE20_1_REFCLKN
H32 REFCLKP_WIFI 28
H33 REFCLKN_WIFI 28

PCIE20_1_TXP/SATA30_1_TXP
PCIE20_1_TXN/SATA30_1_TXN
K33 PCIE20_1_TXP C207 1 — 2 NA X5R 6.3V C0402 — PCIE20_1_TXP_WIFI 28
K34 PCIE20_1_TXN C206 1 — 2 NA X5R 6.3V C0402 — PCIE20_1_TXN_WIFI 28

PCIE20_1_RXP/SATA30_1_RXP
PCIE20_1_RXN/SATA30_1_RXN
J33 C205 1 — 2 NA X5R 6.3V C0402 — PCIE20_1_RXP_WIFI 28
J34 C204 1 — 2 NA X5R 6.3V C0402 — PCIE20_1_RXN_WIFI 28

VDDA_0V85
PCIE20_SATA30_1_AVDD_0V85
L28 — C600 NA X5R 6.3V C0201 — C580 NA X5R 10V C0402

PCIE20_SATA30_1_AVDD_1V8
L27 — C618 NA X5R 6.3V C0201 — C668 NA X5R 10V C0402 — VCCA_1V8

PCIE20/SATA30/USB30 OTG Mux2

PCIe30x1_1
1Lane(RC)--3(1L1)

SATA30 HOST
Controller2

USB30 OTG
Controller2

MUX

PCIE20:Gen1/Gen2
USB 30:Gen1
SATA30:Gen1/Gen2/Gen3

TO PCIE 2.5G RJ45

PCIE20_2_REFCLKP
PCIE20_2_REFCLKN
G31 REFCLKP_100M_RJ45 30
G30 REFCLKN_100M_RJ45 30

PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP
PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN
H30 PCIE20_2_TXP 30
H29 PCIE20_2_TXN 30

PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP
PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN
J31 PCIE20_2_RXP 30
J30 PCIE20_2_RXN 30

PCIE20_SATA30_USB30_2_AVDD_0V85
K28 — C627 NA X5R 6.3V C0201 — C579 NA X5R 10V C0402 — VDDA_0V85

PCIE20_SATA30_USB30_2_AVDD_1V8
K27 — C612 NA X5R 6.3V C0201 — C323 NA X5R 10V C0402 — VCCA_1V8

NA

Note:
Merge the two mipi csi's power need 1X105+1X104 cap.

RK3588_O(PCIE30)

Note:
Only PCIE30 Controller 0 support RC and EP,Other controller only support RC Mode.

CLK Differential Pair:
100 Ohm ±10%
DATA Differential Pair:
PCIE30: 85 Ohm ±10%

U15O

PCIE30X4

PCIe30X4
4Lane(DM)--0(4L)

PCIe30x1_0
1Lane(RC)--2(1L0)

PCIe30x2
2Lane(RC)--1(2L)

PCIe30x1_1
1Lane(RC)--3(1L1)

PCIE30:
PCIe1.1(2.5Gbps)
PCIe2.1(5Gbps)
PCIe3.0(8Gbps)

PCIE20/SATA30 MUX1

PCIE20/SATA30/USB30 MUX2

NA

PCIE30 PORT0 DM(EP&RC)

PCIE30_PORT0_REF_CLKP
PCIE30_PORT0_REF_CLKN

Lane0
PCIE30_PORT0_TX0P
PCIE30_PORT0_TX0N
PCIE30_PORT0_RX0P
PCIE30_PORT0_RX0N

Lane1
PCIE30_PORT0_TX1P
PCIE30_PORT0_TX1N
PCIE30_PORT0_RX1P
PCIE30_PORT0_RX1N

PCIE30_PORT0_RESREF
B34 PCIE30_0_REF R164 1 — R0201 — 2 NA 1%

PCIE30_PORT0_AVDD0V75
G24 — VDDA_0V75
C359 NA X5R 6.3V C0201 — C617 NA X5R 10V C0402

PCIE30_PORT0_AVDD1V8
G23 — VCCA_1V8
C611 NA X5R 6.3V C0201 — C667 NA X5R 10V C0402

E33 PCIE30_PORT0_REFCLKP_IN 32
E34 PCIE30_PORT0_REFCLKN_IN 32
D32 PCIE30_PORT0_TX0P 32
D33 PCIE30_PORT0_TX0N 32
G33 PCIE30_PORT0_RX0P 32
G34 PCIE30_PORT0_RX0N 32
C33 PCIE30_PORT0_TX1P 32
C34 PCIE30_PORT0_TX1N 32
F32 PCIE30_PORT0_RX1P 32
F33 PCIE30_PORT0_RX1N 32

PCIE30 PORT1 (RC)

PCIE30_PORT1_REF_CLKP
PCIE30_PORT1_REF_CLKN

Lane2
PCIE30_PORT1_TX0P
PCIE30_PORT1_TX0N
PCIE30_PORT1_RX0P
PCIE30_PORT1_RX0N

Lane3
PCIE30_PORT1_TX1P
PCIE30_PORT1_TX1N
PCIE30_PORT1_RX1P
PCIE30_PORT1_RX1N

PCIE30_PORT1_RESREF
A33 PCIE30_1_REF R166 1 — R0201 — 2 NA 1%

PCIE30_PORT1_AVDD0V75
H24 — VDDA_0V75
C619 NA X5R 6.3V C0201 — C360 NA X5R 10V C0402

PCIE30_PORT1_AVDD1V8
H23 — VCCA_1V8
C610 NA X5R 6.3V C0201 — C658 NA X5R 10V C0402

A28 PCIE30_PORT1_REFCLKP_IN 32
B28 PCIE30_PORT1_REFCLKN_IN 32
B30 PCIE30_PORT1_TX2P 32
A30 PCIE30_PORT1_TX2N 32
B32 PCIE30_PORT1_RX2P 32
A32 PCIE30_PORT1_RX2N 32
C29 PCIE30_PORT1_TX3P 32
B29 PCIE30_PORT1_TX3N 32
C31 PCIE30_PORT1_RX3P 32
B31 PCIE30_PORT1_RX3N 32

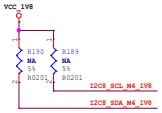
Note:
The Caps to the left of green line should be placed under the U1000 package.Other caps should be placed close to the U1000 package.

Note:
Merge the two mipi csi's power need 1X105+1X104 cap.

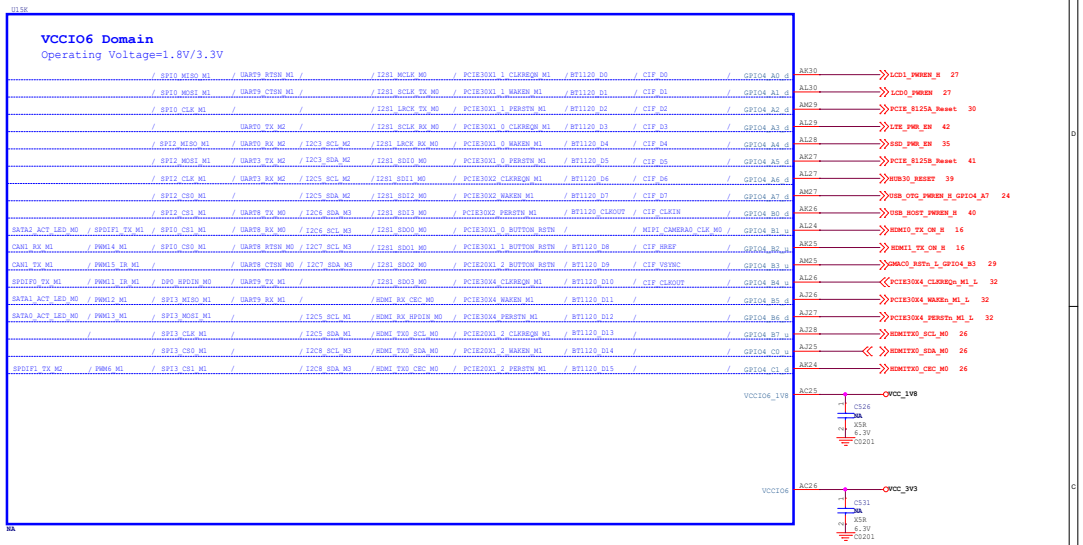
HINLINK			
Project:	H88K_V3.1		
File:	17.RK3588_PCIE30/PCIE20/SATA30		
Date:	Tuesday, June 25, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	17 of 43

RK3588_J(VCCIO5 Domain)

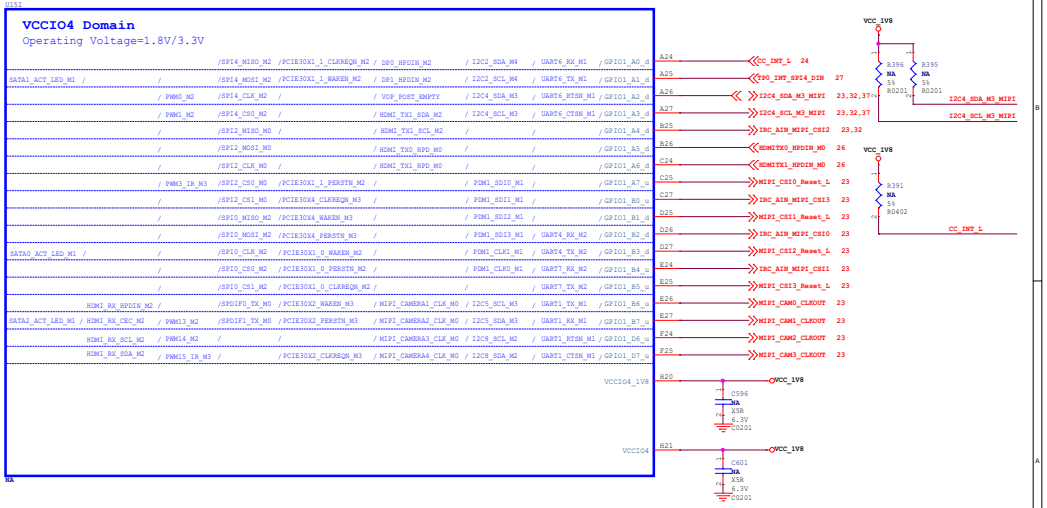
default follow EVB1,different from NVR 3V3



RK3588_K(VCCIO6 Domain)



RK3588_I(VCCIO4 Domain)



HINLINK		
Project:	H88K_V3.1	
File:	18.RK3588_1.8V/ 3.3V GPIO	
Date:	Tuesday, June 25, 2024	Rev: <Revision>
Designer:	<Designer>	Sheet: 18 of 43

PMIC_SPI_CS 10
PMIC_SPI_MOSI 10
PMIC_SPI_CLK 10

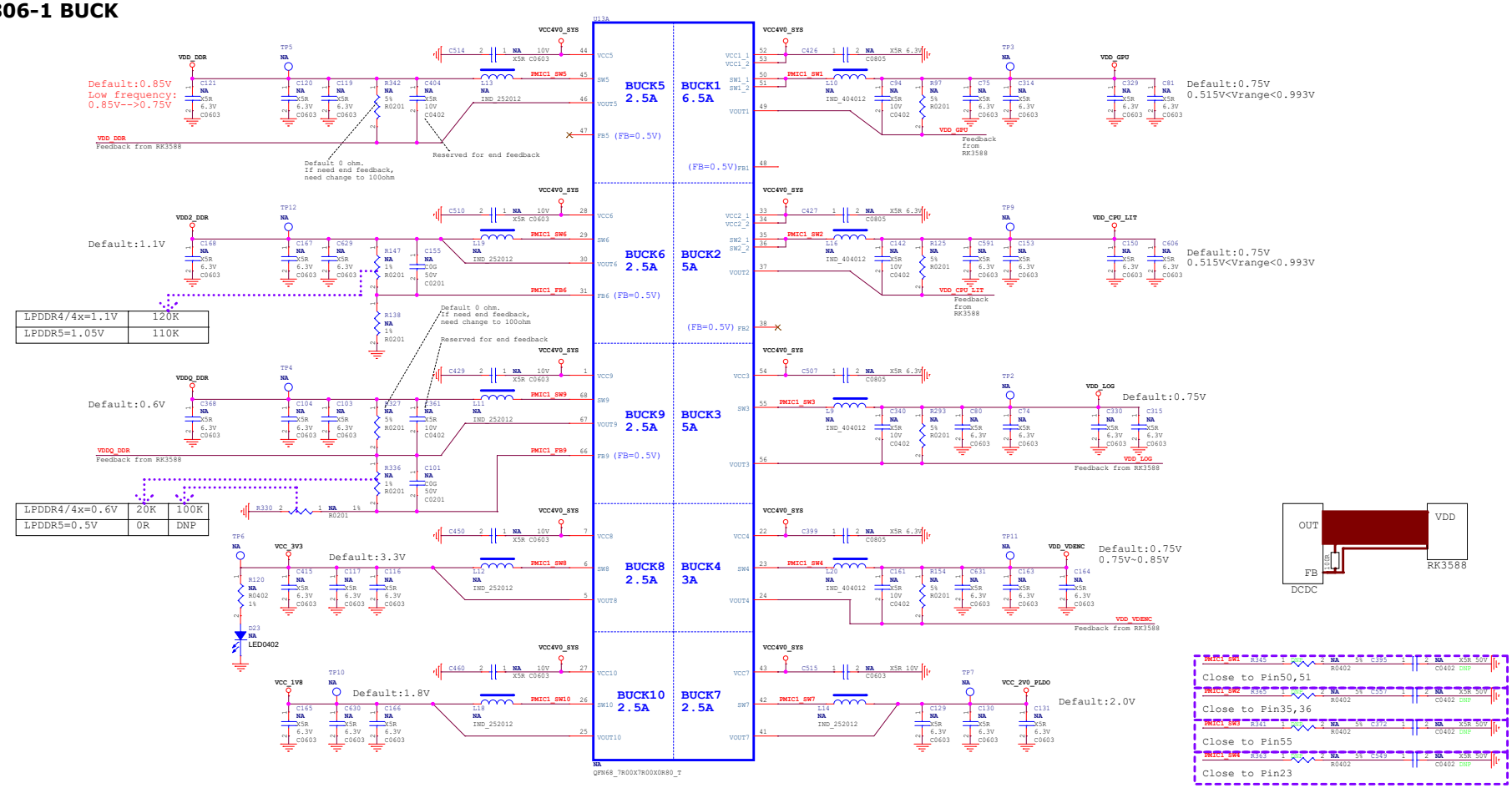
PMIC_PWR_CTRL1 10
PMIC_PWR_CTRL2 10
PMIC_PWR_CTRL3 10

PMIC_INT_L 10

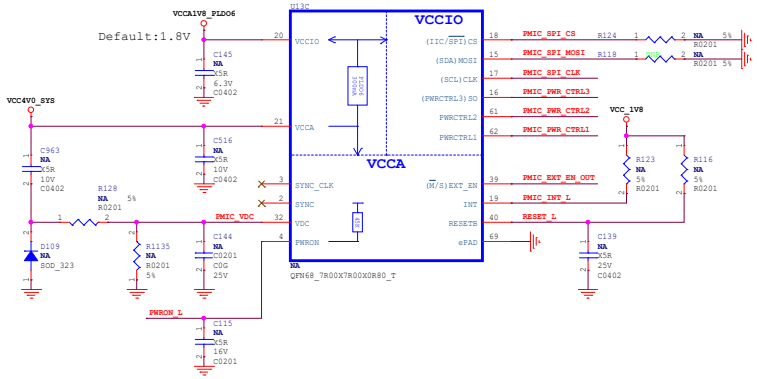
RESET_L 10,36
PWRON_L 36

PMIC_EXT_EN_OUT 20

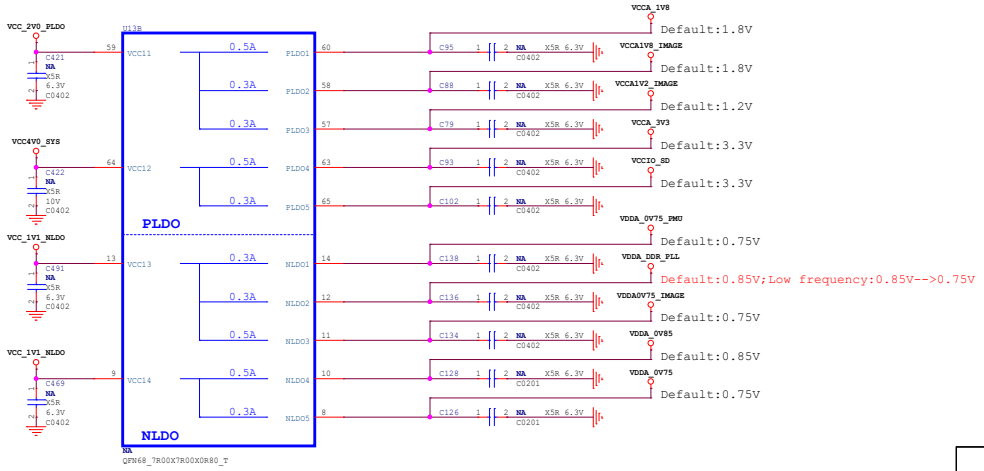
PMIC RK806-1 BUCK



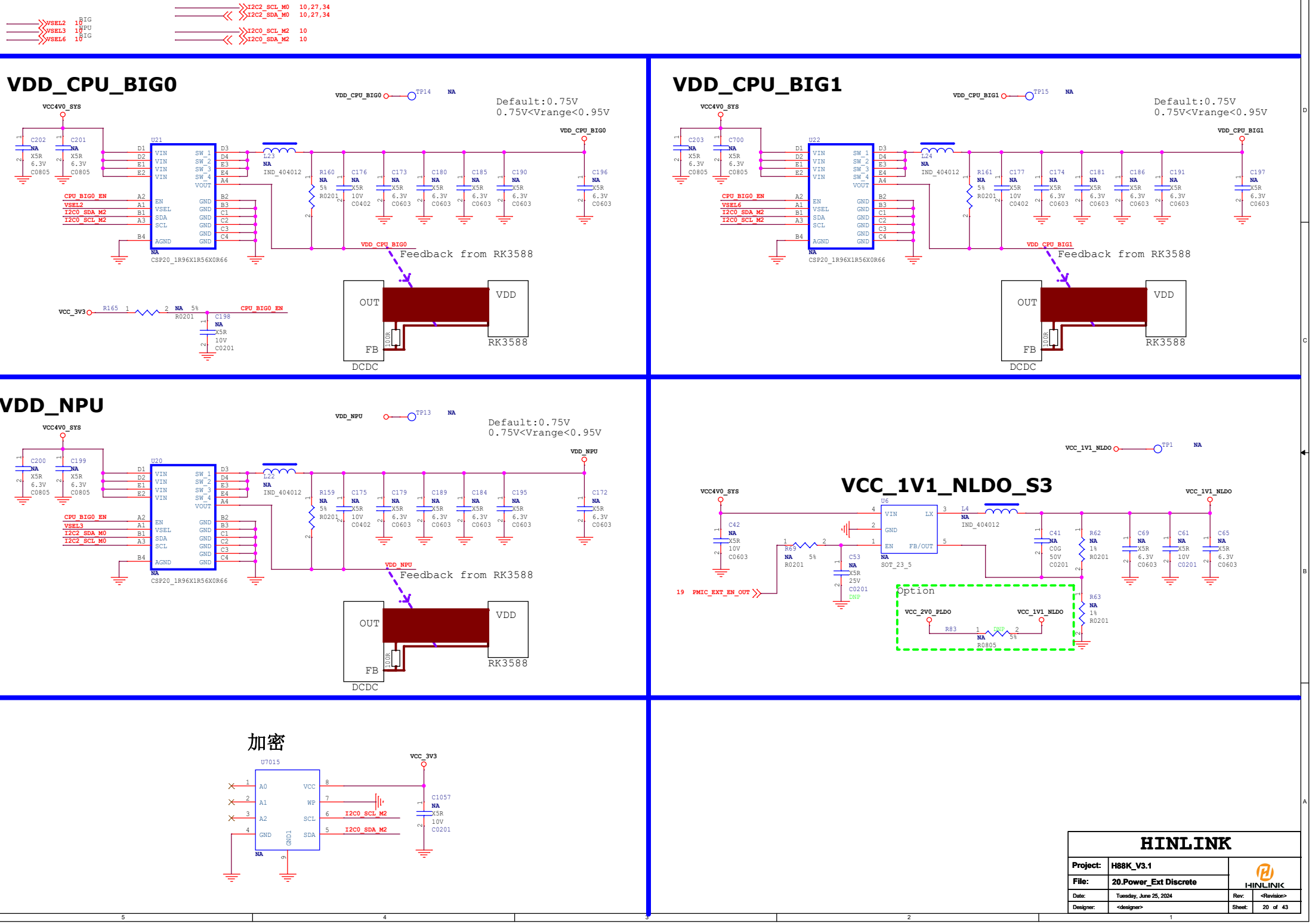
PMIC RK806-1 Managerment



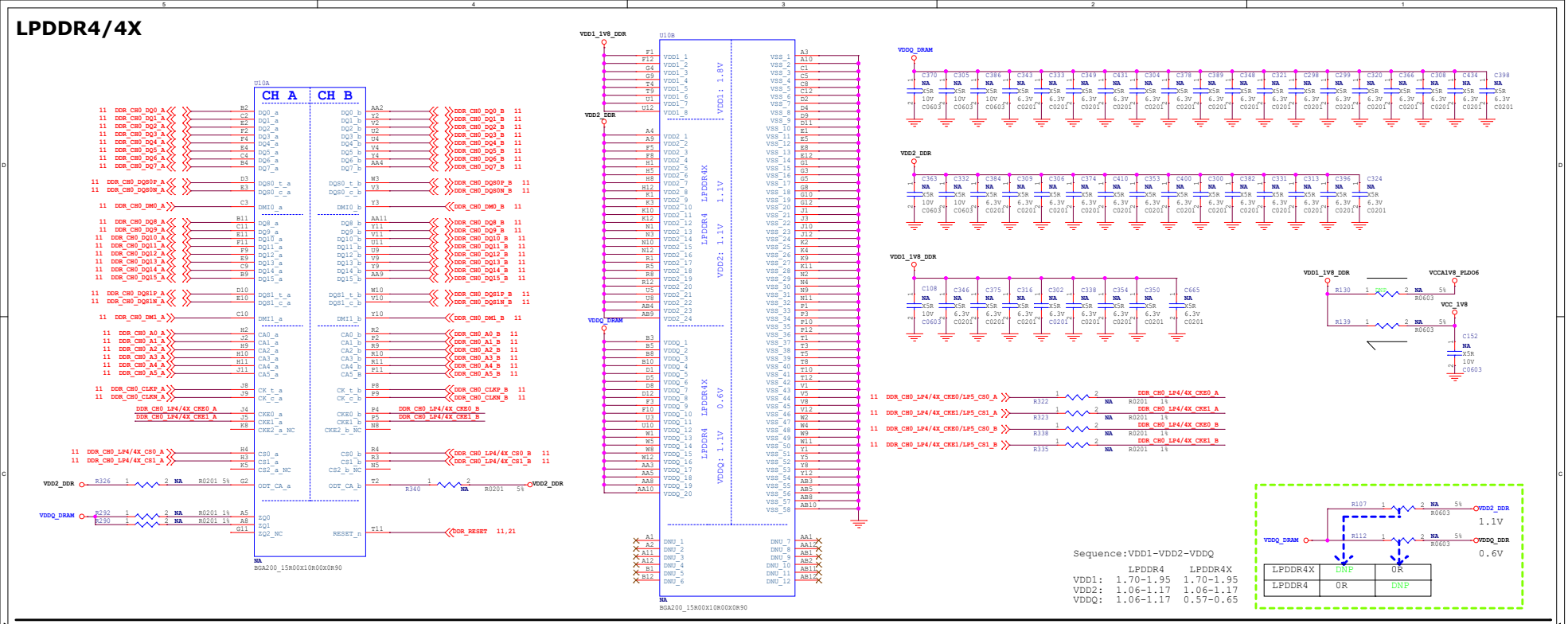
PMIC RK806-1 LDO

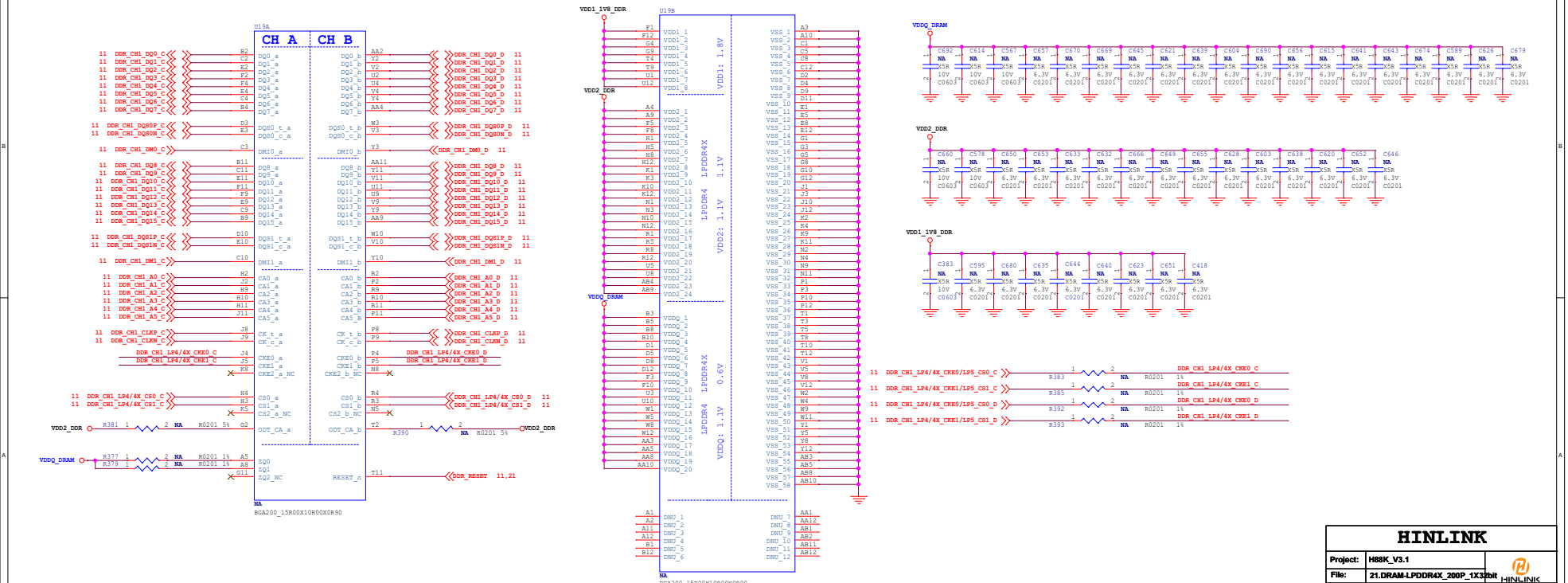


HINLINK			
Project:	H88K_V3.1		
File:	19.Power-PMIC_RK806-1		
Date:	Tuesday, June 25, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	19 of 43


VSEL2 10 BIG
VSEL3 10 CPU
VSEL6 10 BIG
I2C2_SCL_M0 10,27,34
I2C2_SDA_M0 10,27,34
I2C0_SCL_M2 10
I2C0_SDA_M2 10
VDD_CPU_BIG0
Default:0.75V
0.75V<Vrange<0.95V
VCC4V0_SYS
CPU_BIG0_EN
VSEL2
I2C0_SDA_M2
I2C0_SCL_M2
CSP20_1R96X1R56X0R66
Feedback from RK3588
OUT
VDD
FB
RK3588
DCDC
VCC_3V3
VDD_CPU_BIG1
VSEL6
VDD_NPU
VSEL3
I2C2_SDA_M0
I2C2_SCL_M0
VCC_1V1_NLDO
VCC_1V1_NLDO_S3
PMIC_EXT_EN_OUT
Option
VCC_2V0_PLDO
加密
U7015
I2C0_SCL_M2
I2C0_SDA_M2
HINLINK
Project: H88K_V3.1
File: 20.Power_Ext Discrete
Date: Tuesday, June 25, 2024
Designer: <designer>
Rev: <Revision>
Sheet: 20 of 43

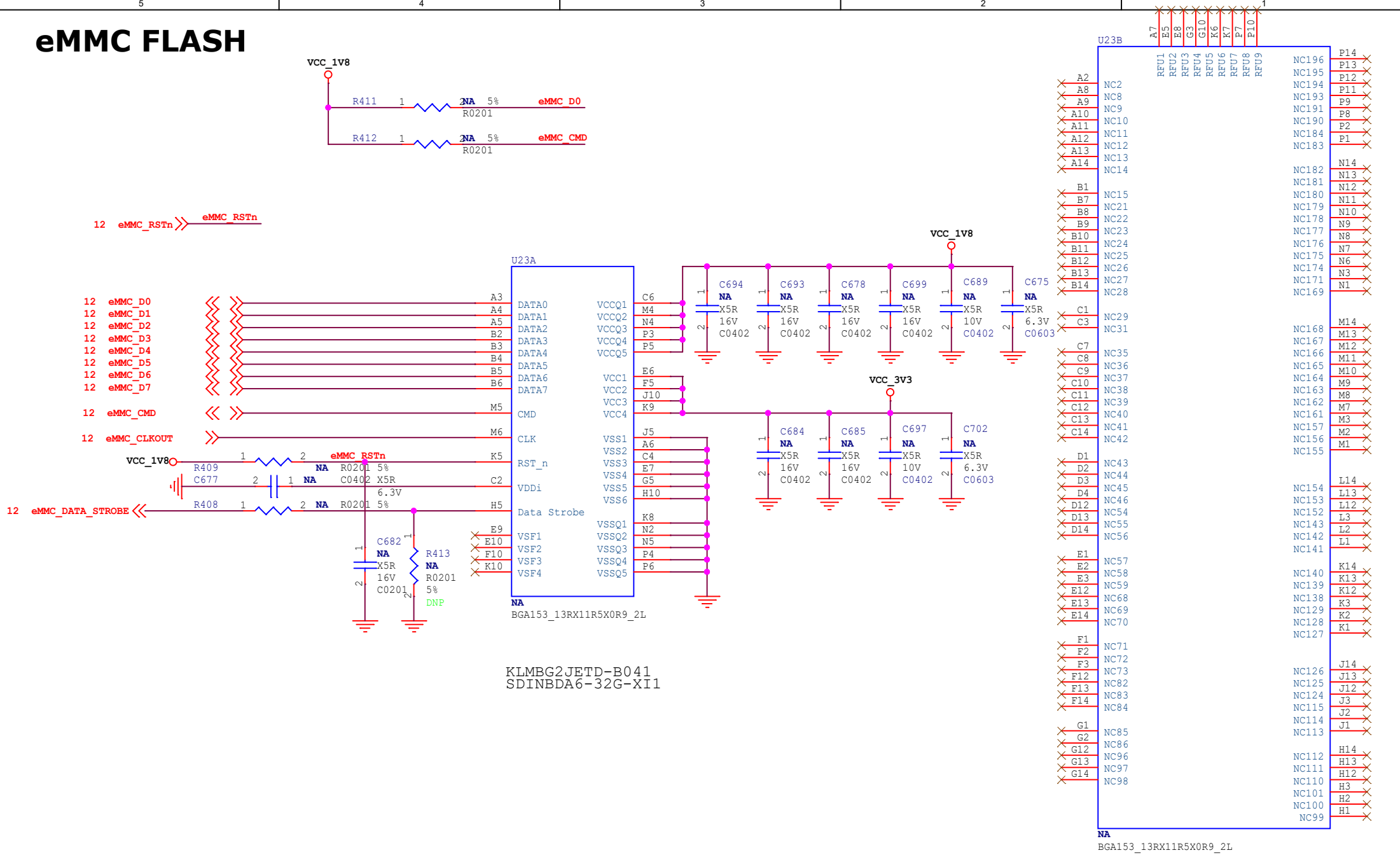
LPDDR4/4X





HINLINK		
Project:	H88K_V3.1	
File:	21.DRAM-LPDDR4X_200P_1X32bit	HINLINK
Date:	Tuesday, June 25, 2024	Rev: <Revision>
Designer:	<Designer>	Sheet: 21 of 43

eMMC FLASH



KLMBG2JETD-B041
SDINBDA6-32G-XI1

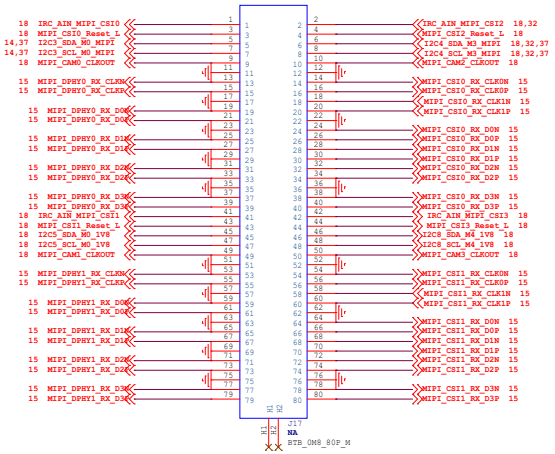
HINLINK			
Project:	H88K_V3.1		
File:	22.Flash-eMMC Flash EVB1		
Date:	Tuesday, June 25, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	22 of 43

MIPI D/C PHY0 CSI_RX

MIPI-CSI0_RX

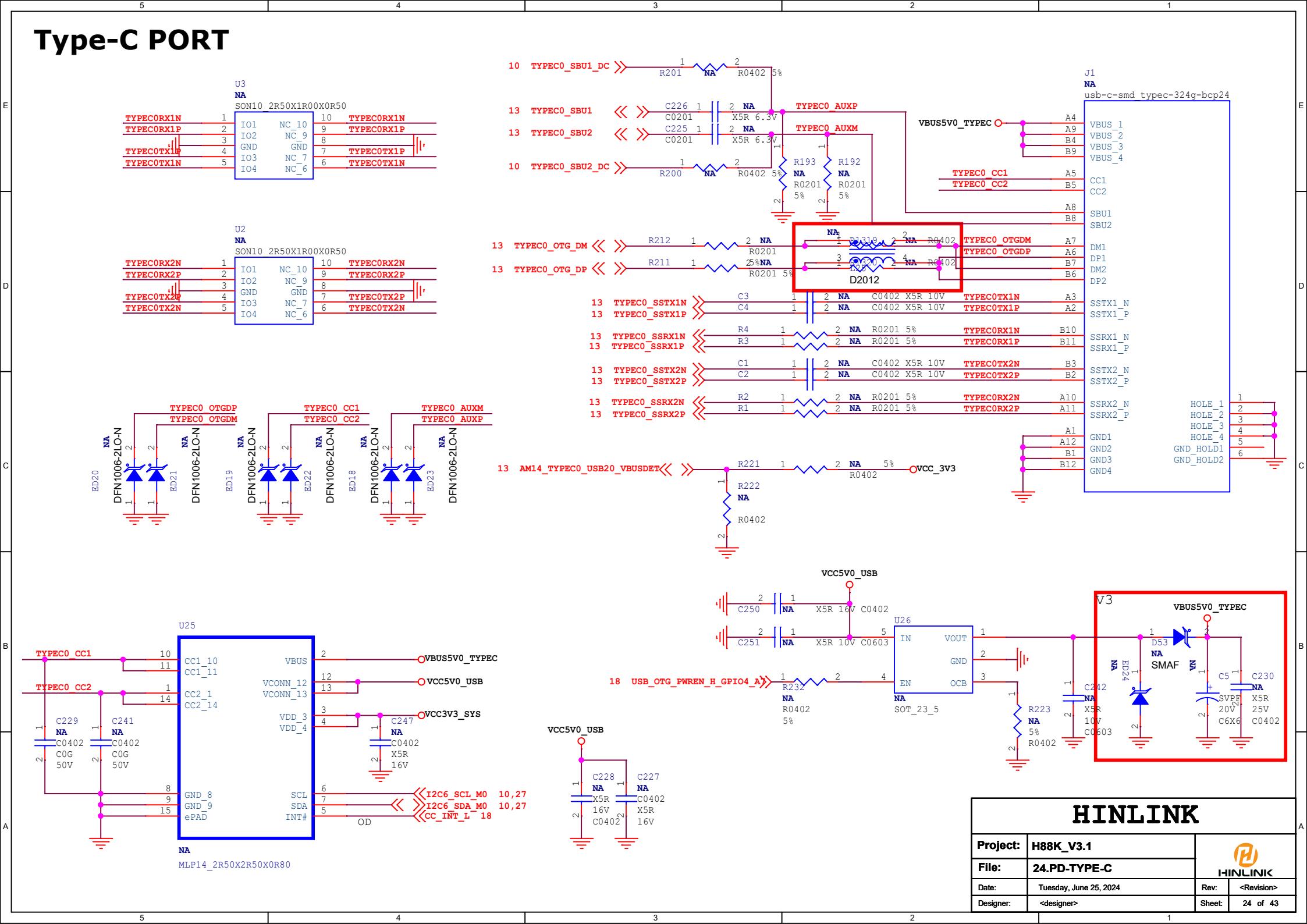
MIPI D/C PHY1 CSI_RX

MIPI-CSI1_RX



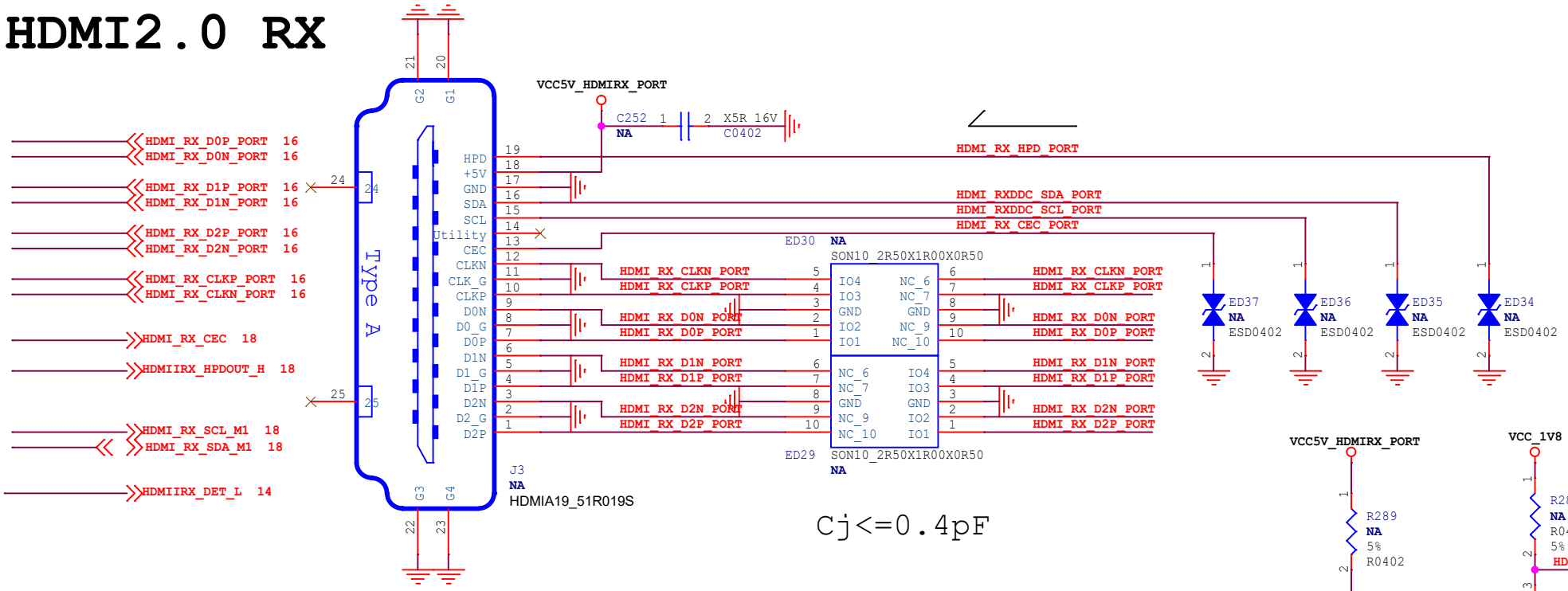
HINLINK		
Project:	H88K_V3.1	HINLINK
File:	23.VI-Camera D/C PHY_RX	
Date:	Tuesday, June 25, 2024	Rev: <Revision>
Designer:	<designer>	Sheet: 23 of 43

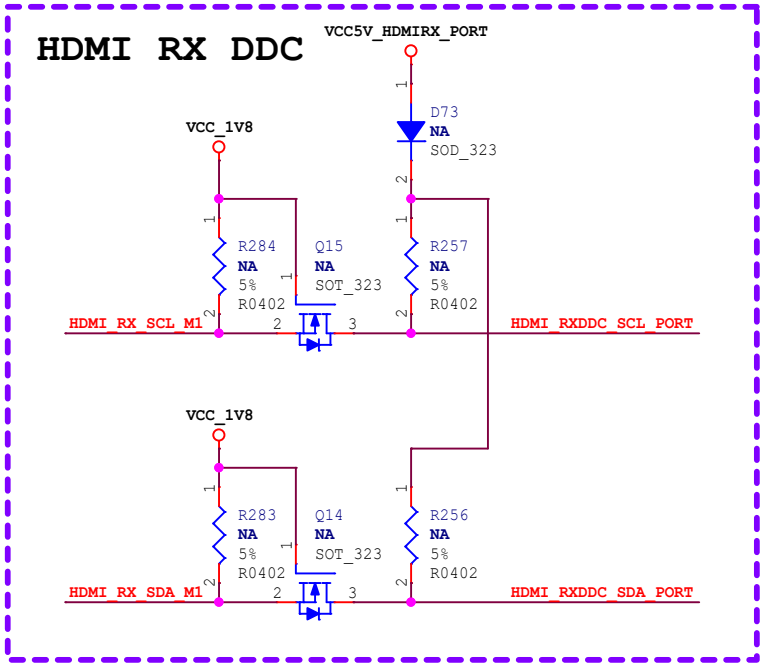
Type-C PORT

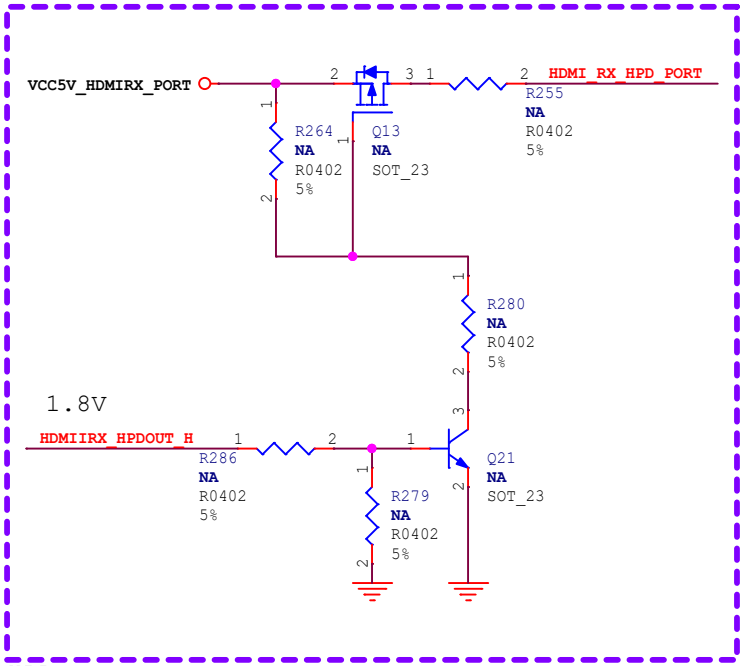


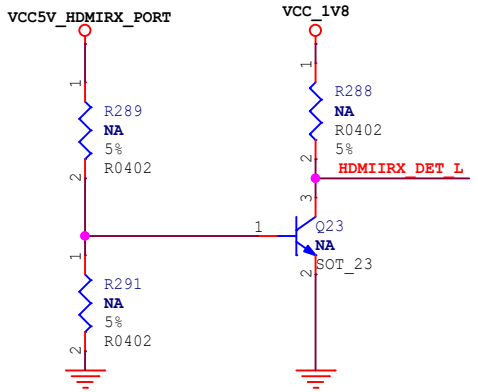
HINLINK			
Project:	H88K_V3.1		
File:	24.PD-TYPE-C		
Date:	Tuesday, June 25, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	24 of 43

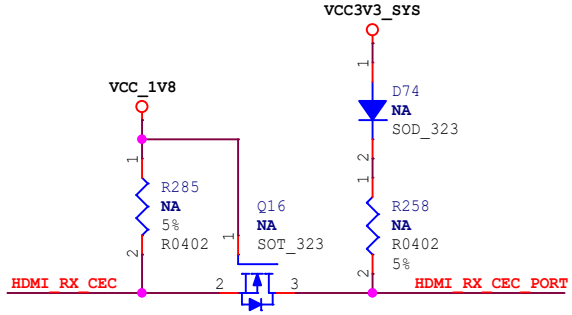
HDMI2.0 RX







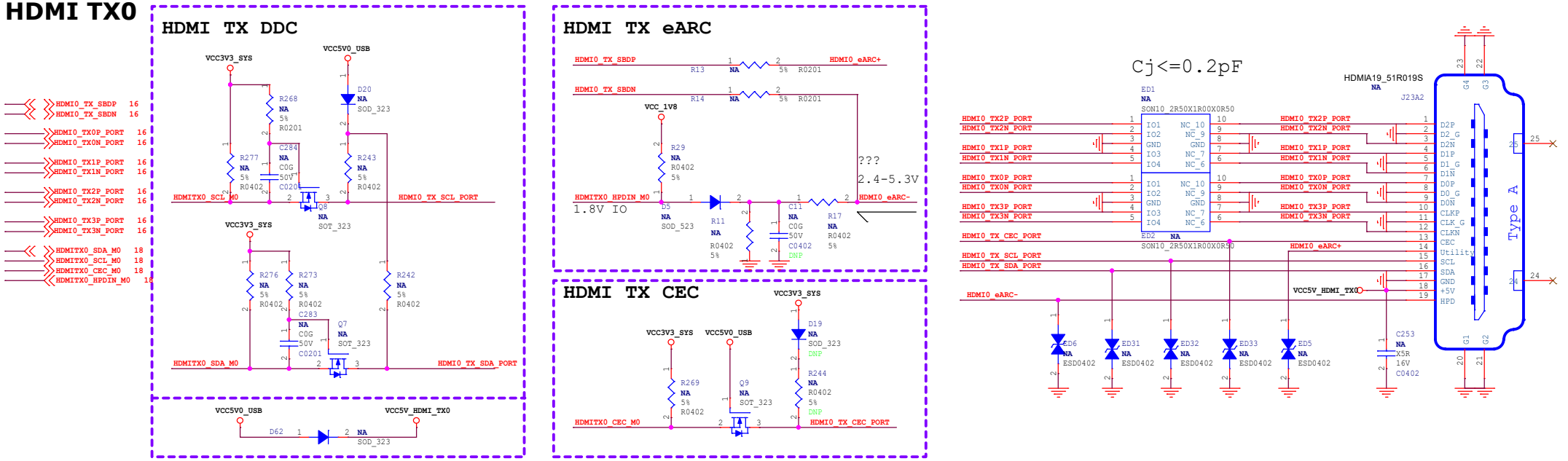




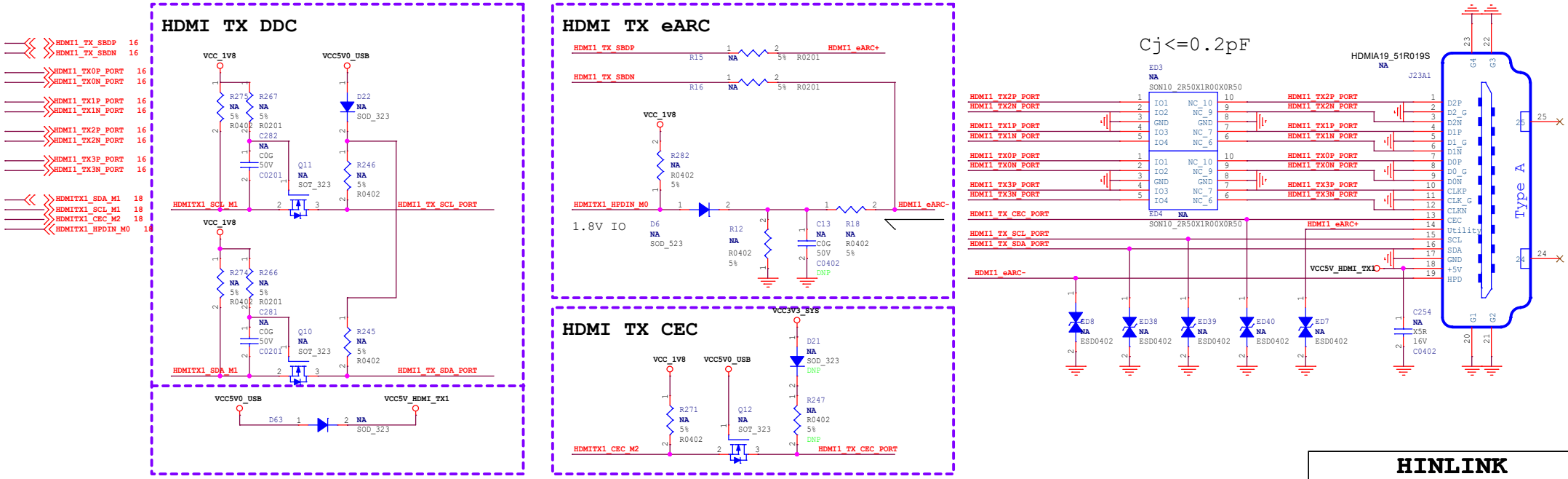
HPD:
Sink Side: Require output, Min 2.4V; Max 5.3V
Source Side:Require input and Detection.
Min 2.0V,Max:5.3V.

HINLINK		
Project:	H88K_V3.1	HINLINK
File:	25.VI-HDMI2.0 RX	
Date:	Tuesday, June 25, 2024	Rev: <Revision>
Designer:	<designer>	Sheet: 25 of 43

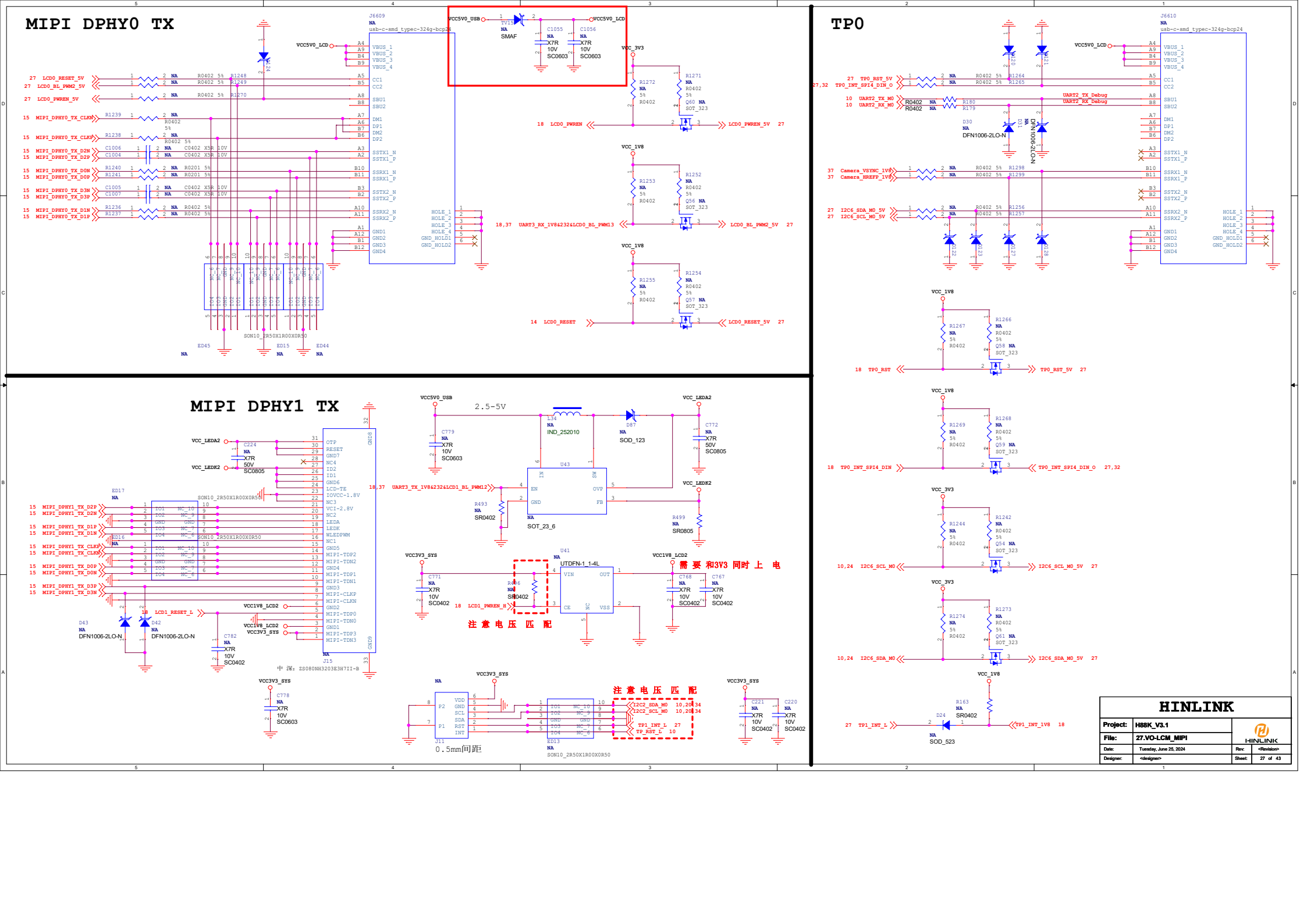
HDMI TX0



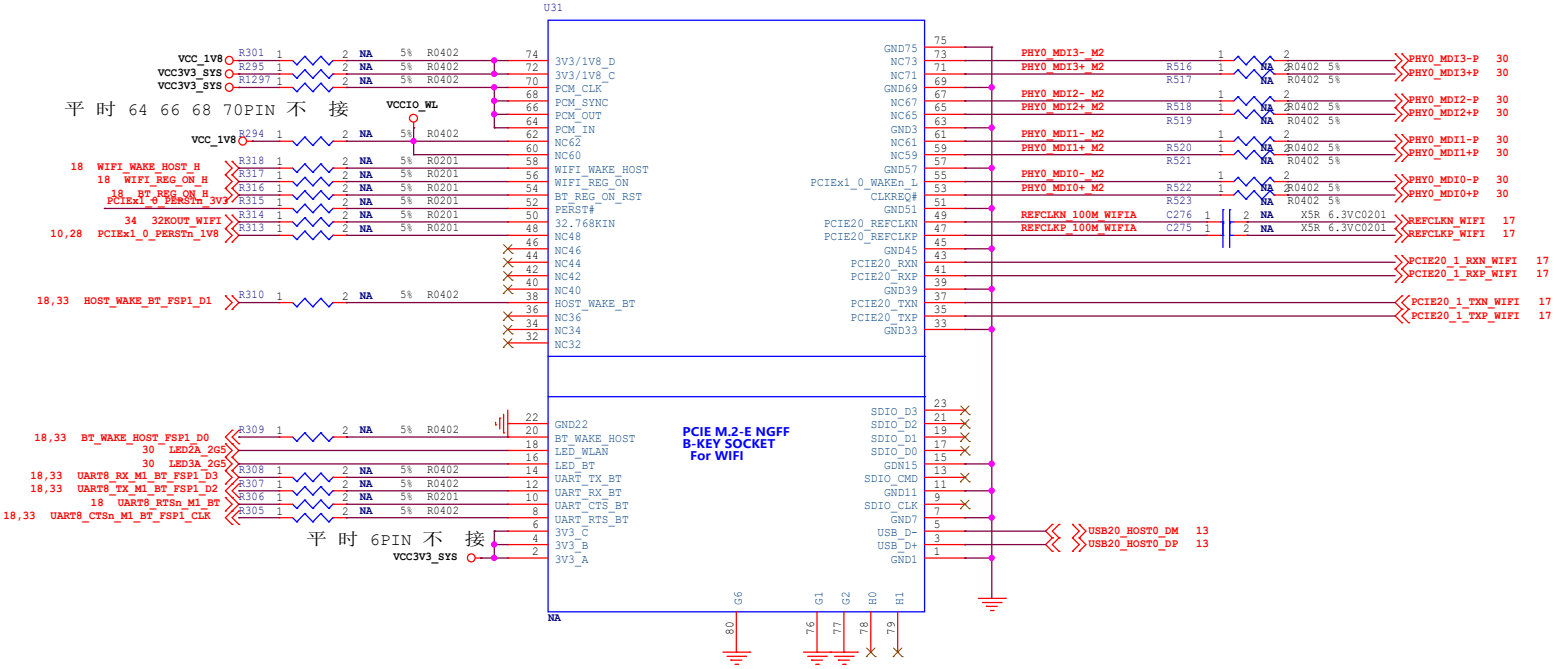
HDMI TX1



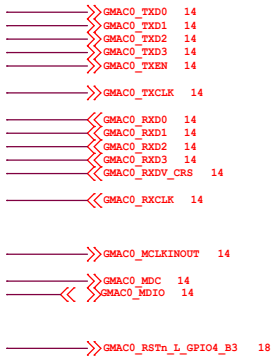
HINLINK		
Project:	H88K_V3.1	HINLINK
File:	26.VO-HDMI2.1 TX	
Date:	Tuesday, June 25, 2024	Rev: <Revision>
Designer:	<designer>	Sheet: 26 of 43

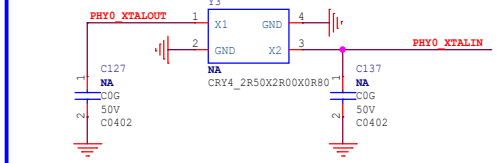

MIPI DPHY0 TX
MIPI DPHY1 TX
TP0
HINLINK
Project: H88K_V3.1
File: 27.VO-LCM_MIPI
Date: Tuesday, June 25, 2024
Designer: <designer>
Rev: <Revision>
Sheet: 27 of 43
注 意 电 压 匹 配
需 要 和3V3 同时 上 电
0.5mm间距

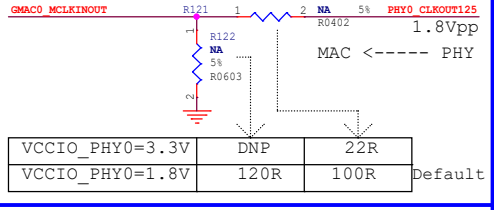
PCIe WIFI6/BT Module-2T2R



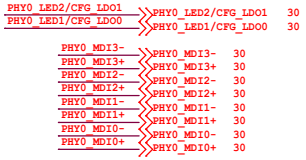
HINLINK			
Project:	H88K_V3.1		
File:	28.WIFI/BT-M2		
Date:	Tuesday, June 25, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	28 of 43

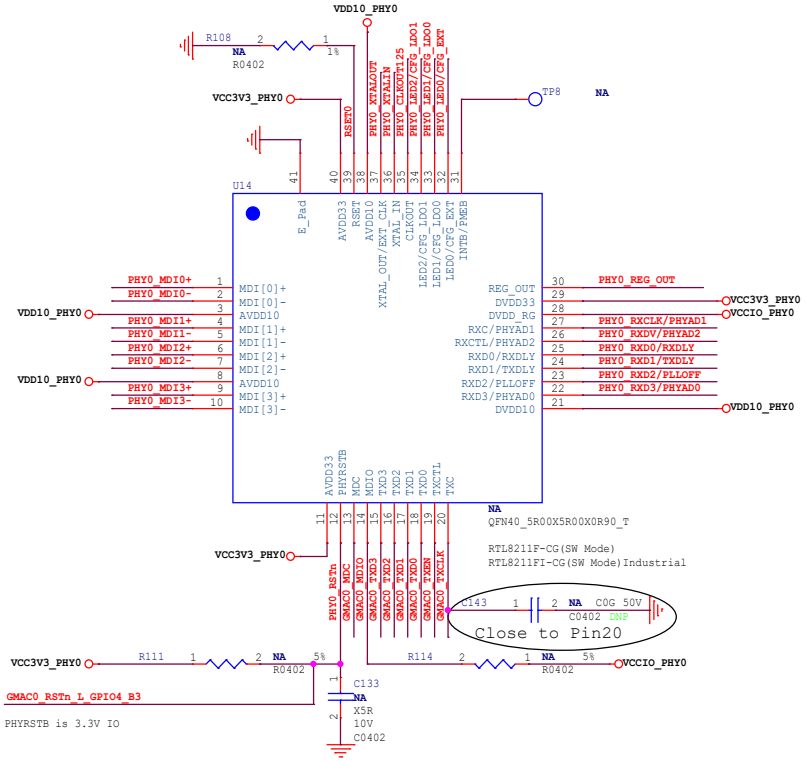


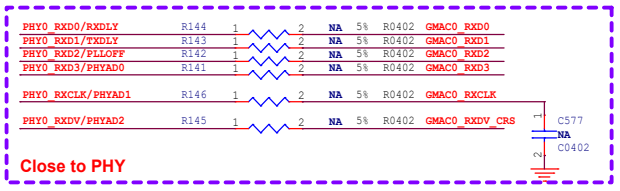


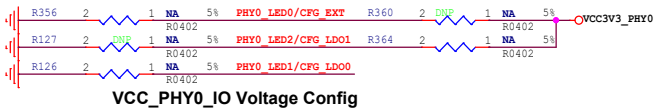


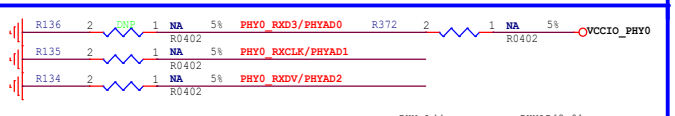
VCCIO_PHY0=3.3V	DNP	22R	
VCCIO_PHY0=1.8V	120R	100R	Default

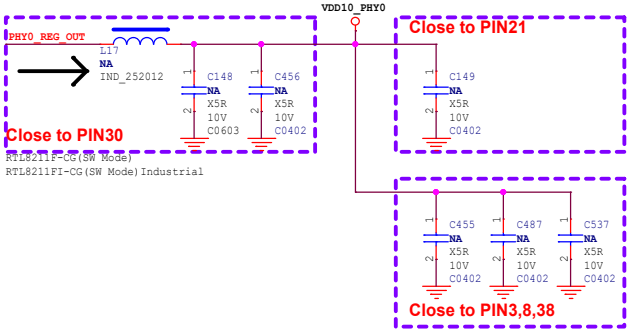




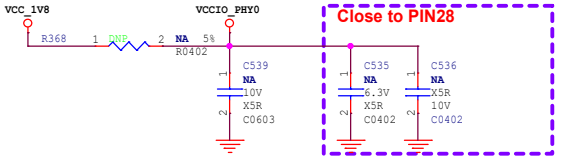


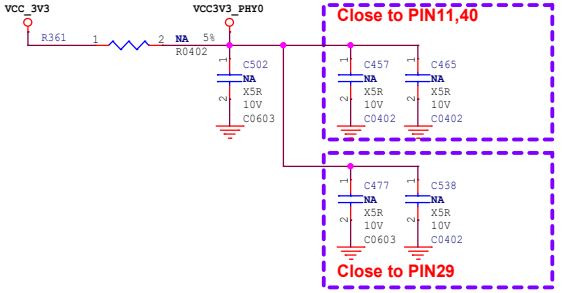






RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V	1'b1	2'b00
External 1.8V	1'b1	2'b10
Internal 1.8V (default)	1'b0	2'b10

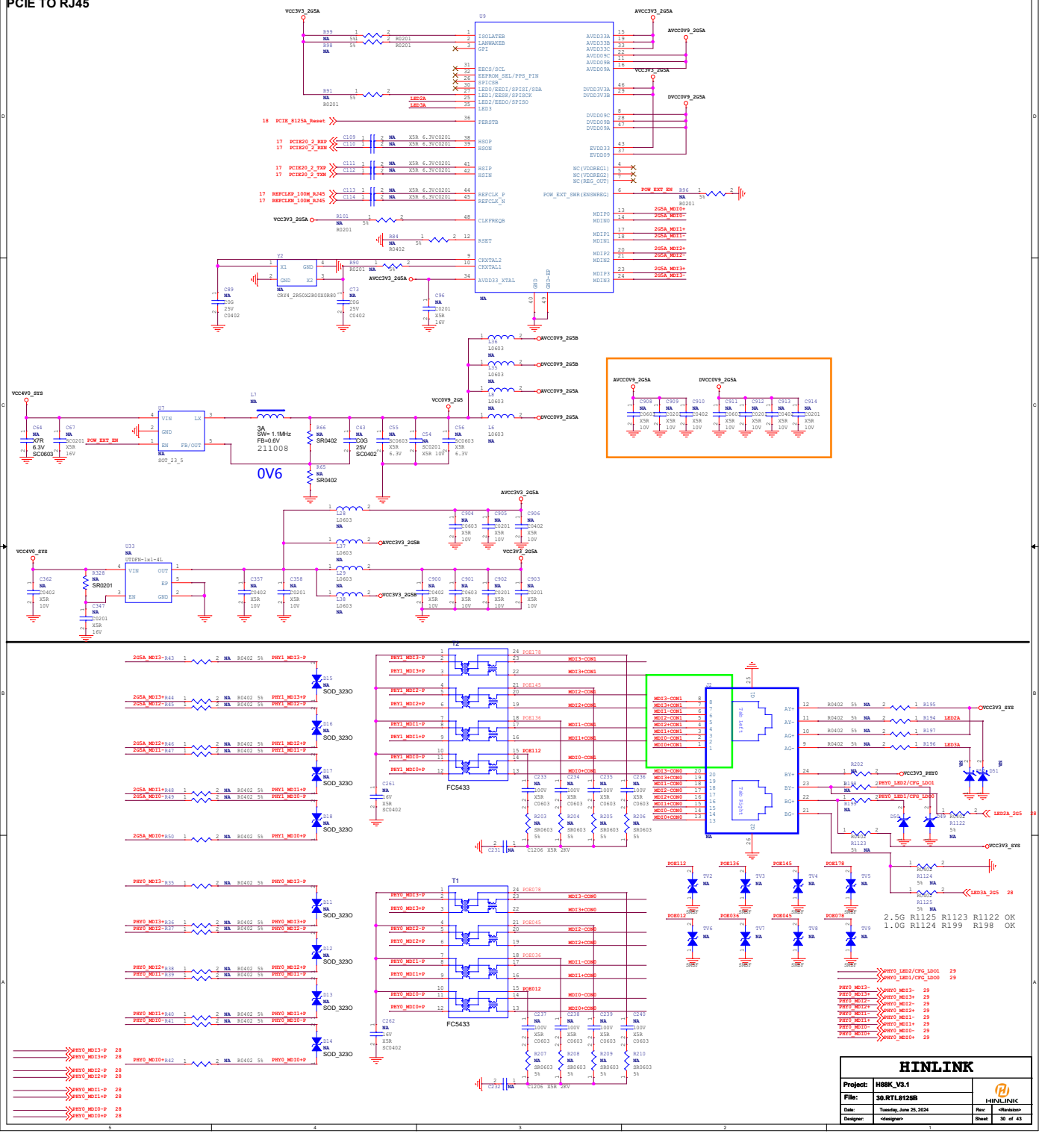




Rockchip Confidential

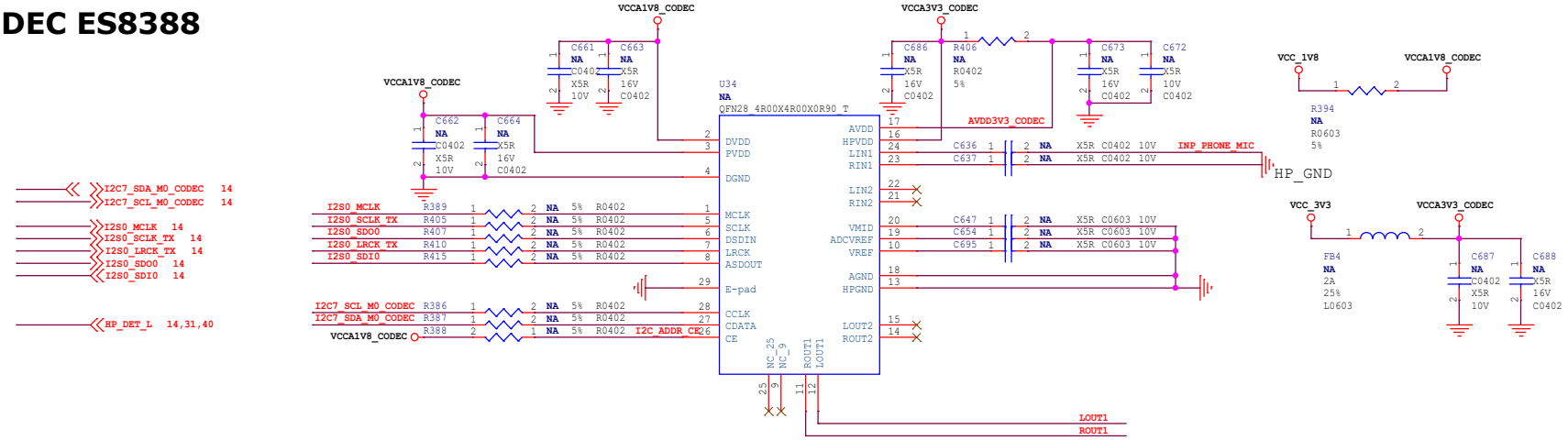
HINLINK		
Project:	H88K_V3.1	
File:	29.RTL8211F	HINLINK
Date:	Tuesday, June 25, 2024	Rev: <Revision>
Designer:	<designer>	Sheet: 29 of 43

PCIE TO RJ45

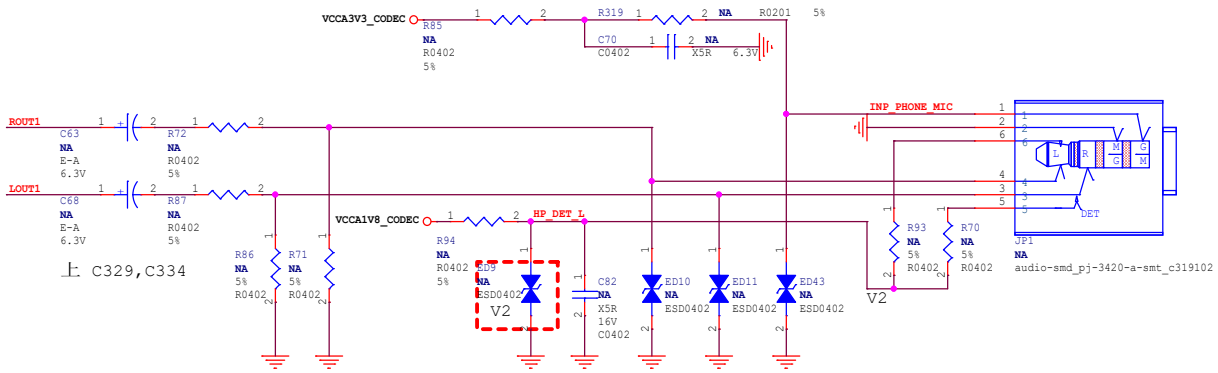


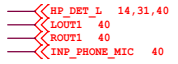
HINLINK			
Project:	H88K_V3.1		
File:	30.RTL8125B		
Date:	Tuesday, June 25, 2024	**Rev:**	<Revision>
Designer:	<designer>	**Sheet:**	30 of 43

CODEC ES8388



EARPHONE



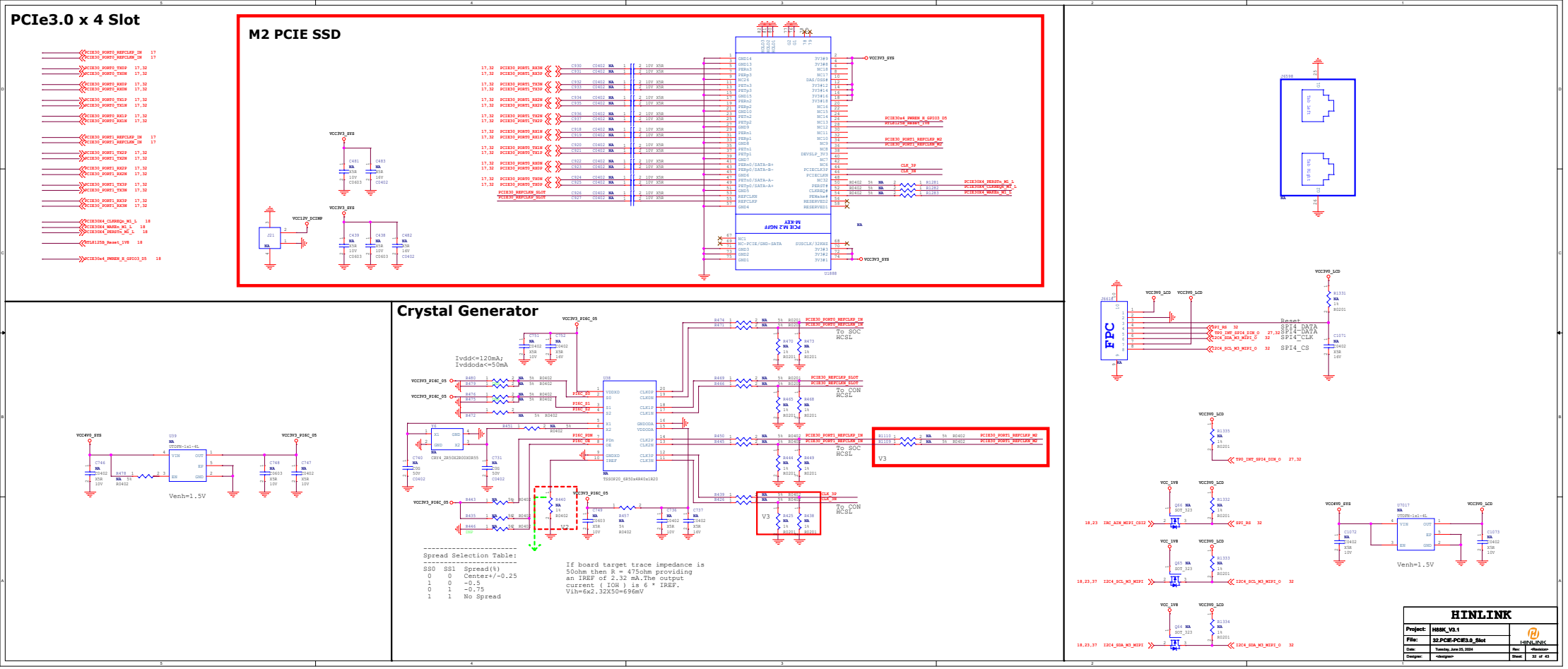


HINLINK		
Project:	H88K_V3.1	
File:	31.Audio Codec-ES8388	
Date:	Tuesday, June 25, 2024	Rev: <Revision>
Designer:	<designer>	Sheet: 31 of 43

PCIe3.0 x 4 Slot

M2 PCIE SSD

Crystal Generator

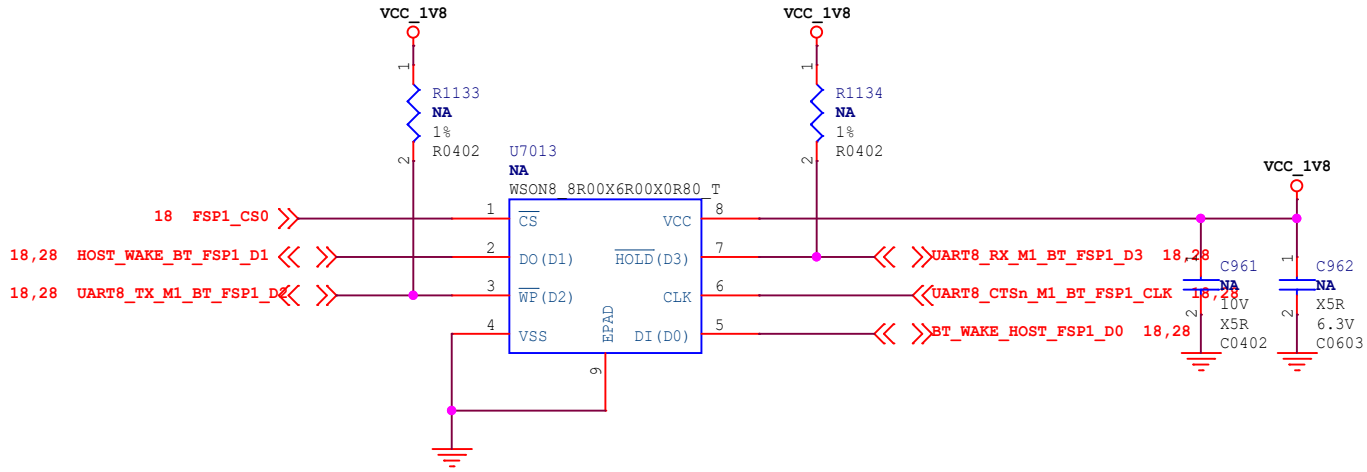


Spread Selection Table:

SS0	SS1	Spread(%)
0	0	Center+/-0.25
1	0	-0.5
0	1	-0.75
1	1	No Spread

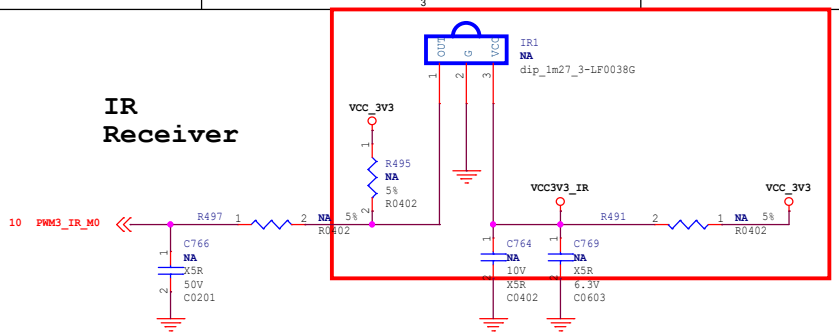
If board target trace impedance is 50ohm then R = 475ohm providing an IREF of 2.32 mA.The output current (IOH) is 6 * IREF.
Vih=6x2.32X50=696mV

HINLINK	
Project:	H88K_V3.1
File:	32.PCIE-PCIE3.0_Slot
Date:	Tuesday, June 25, 2024
Designer:	<Designer>
Rev:	<Revision>
Sheet:	32 of 43

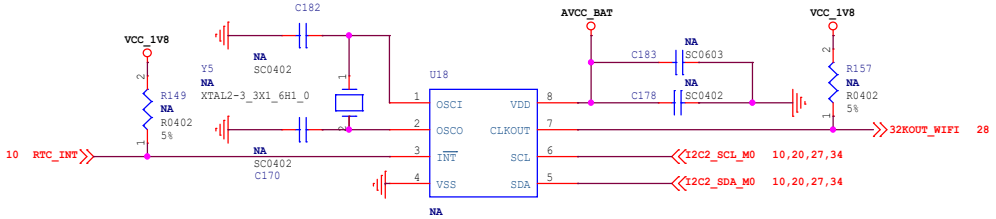


HINLINK			
Project:	H88K_V3.1	HINLINK	
File:	33.NAND_Flash		
Date:	Tuesday, June 25, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	33 of 43

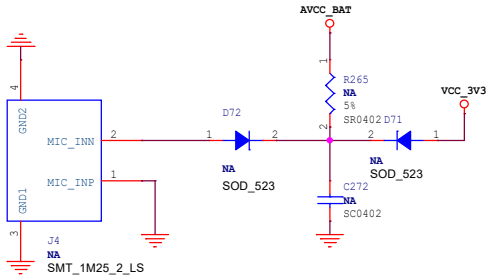
IR Receiver



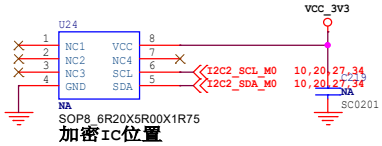
RTC IC



Address:Read A3H,Write A2H

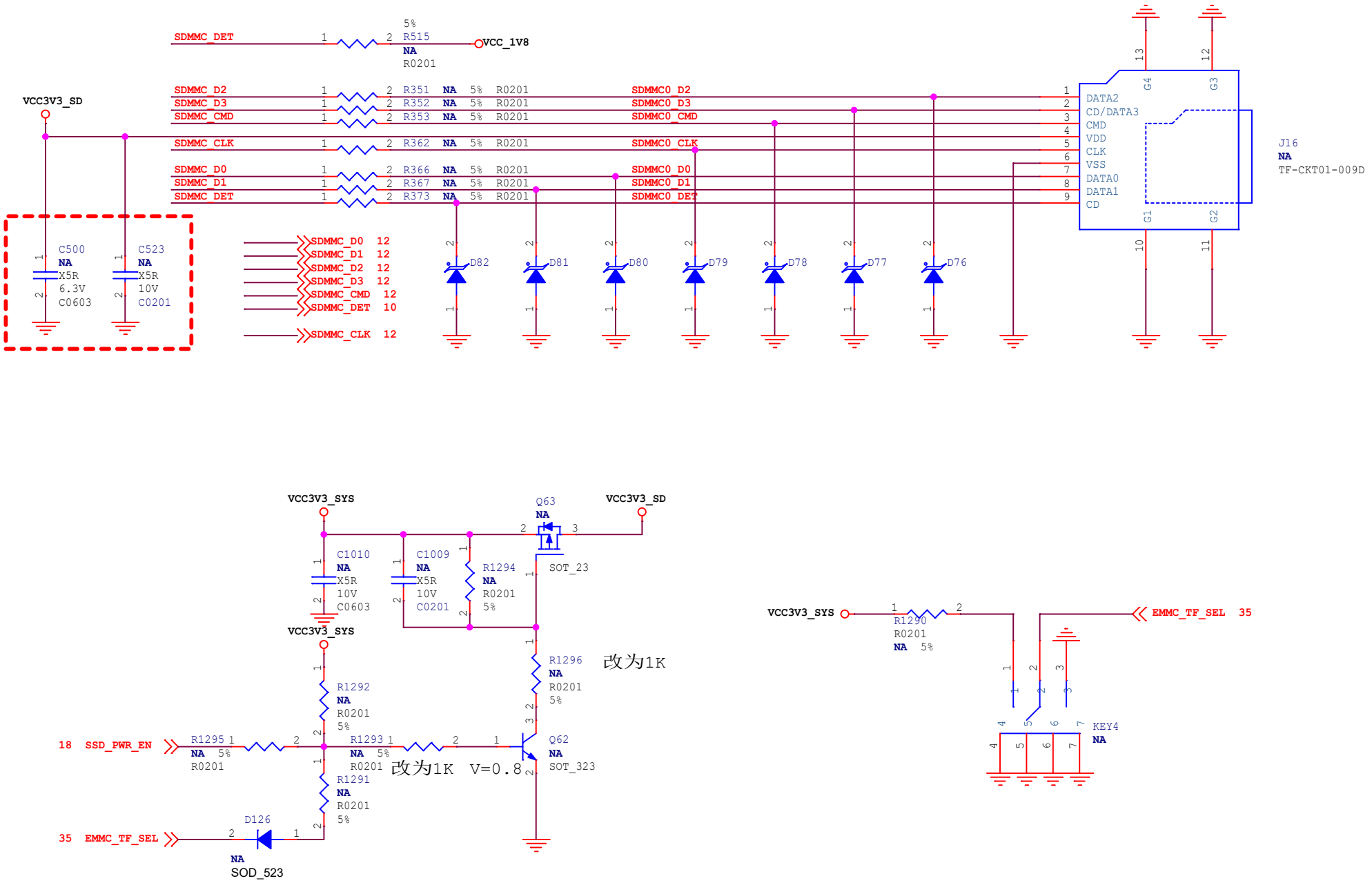


Encryption



加密IC位置

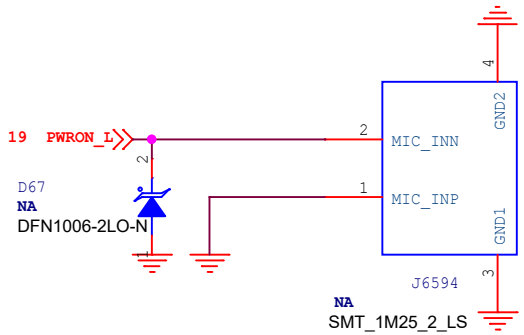
HINLINK			
Project:	H88K_V3.1		
File:	34.IR/RTC		
Date:	Tuesday, June 25, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	34 of 43

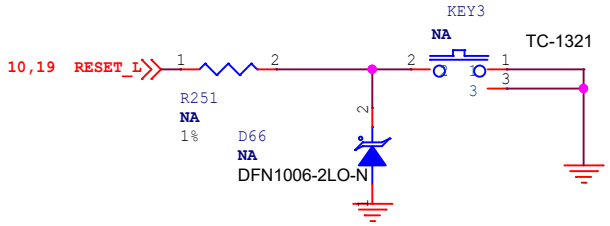


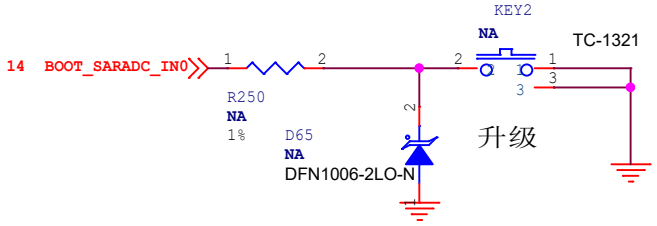
HINLINK			
Project:	H88K_V3.1		
File:	35.SDIO_TF		
Date:	Tuesday, June 25, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	35 of 43

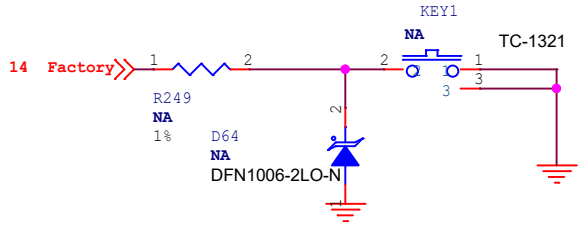
KEY

回复出厂配置



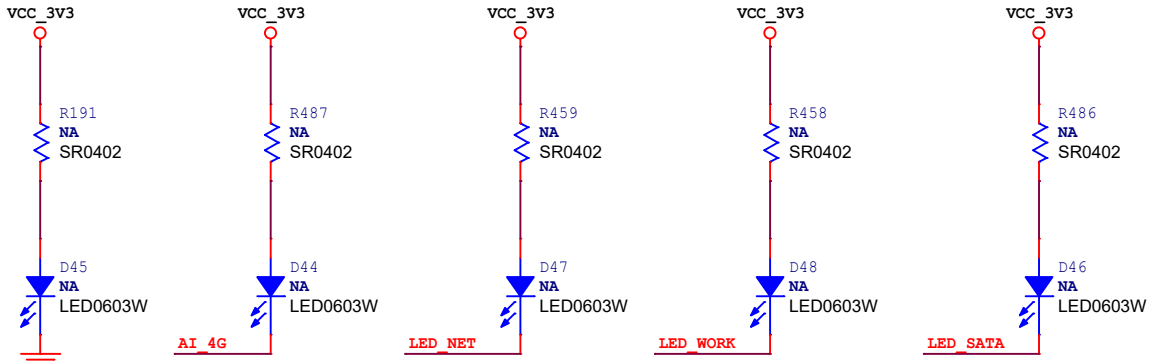




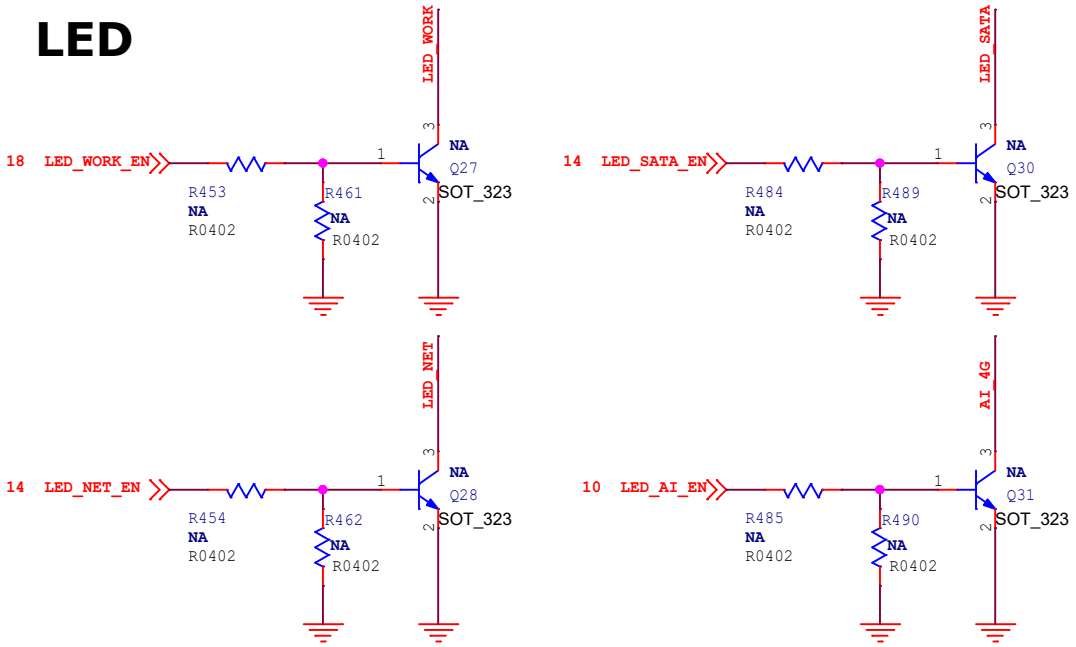


Note:

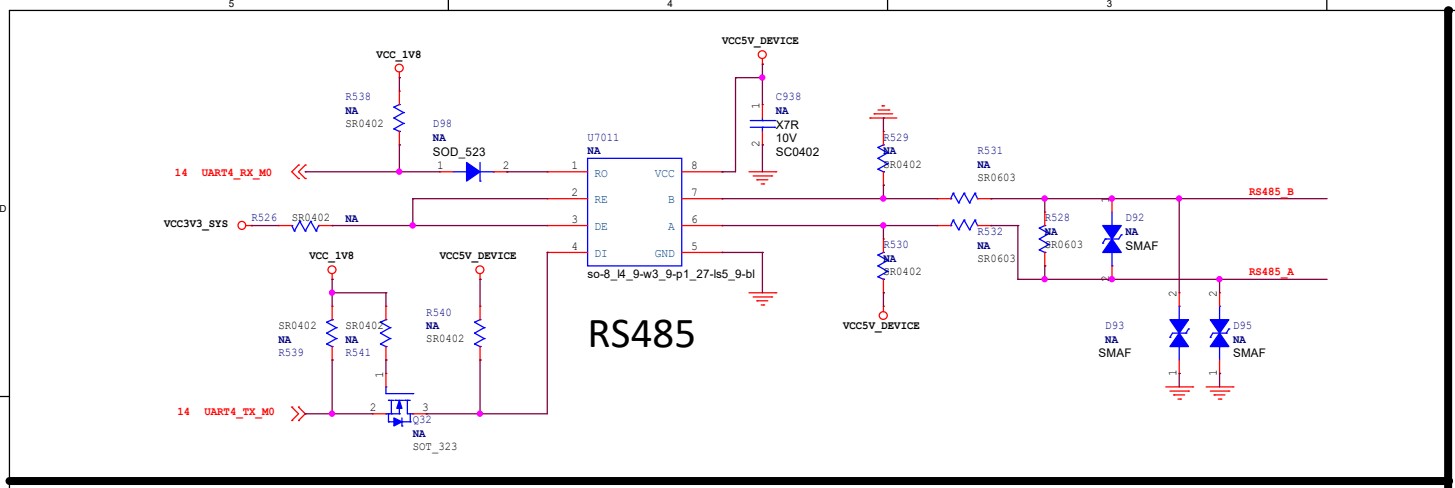
If BOOT_SARADC_IN0=0V after power-on reset, then system will enter into Maskrom mode.

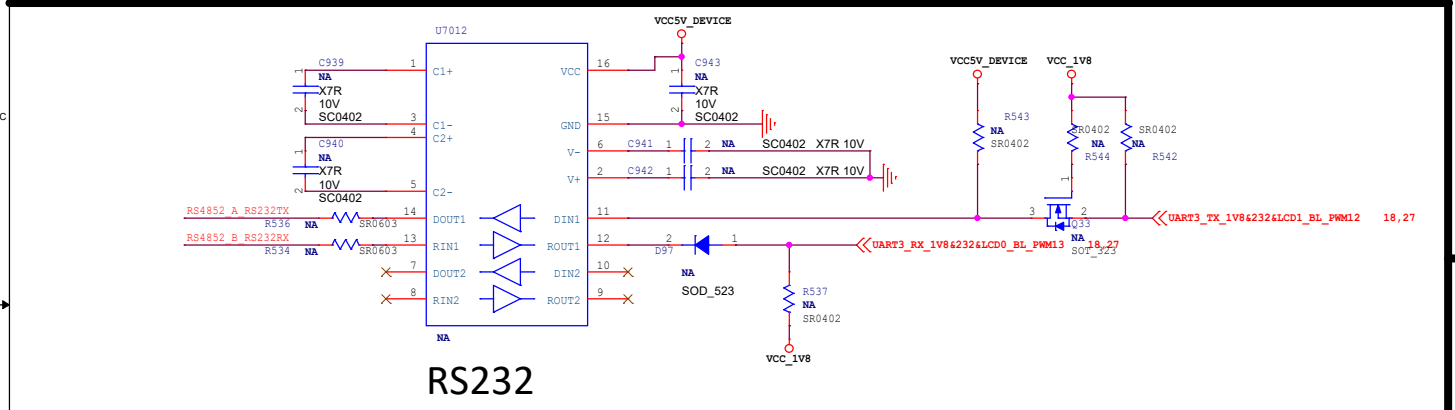


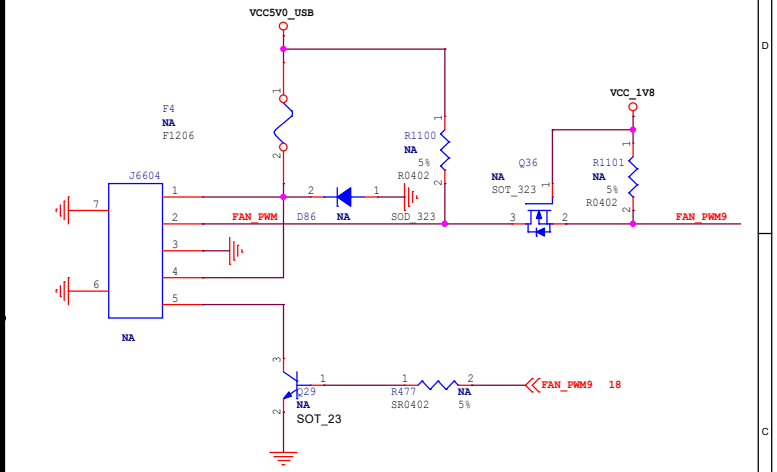
LED

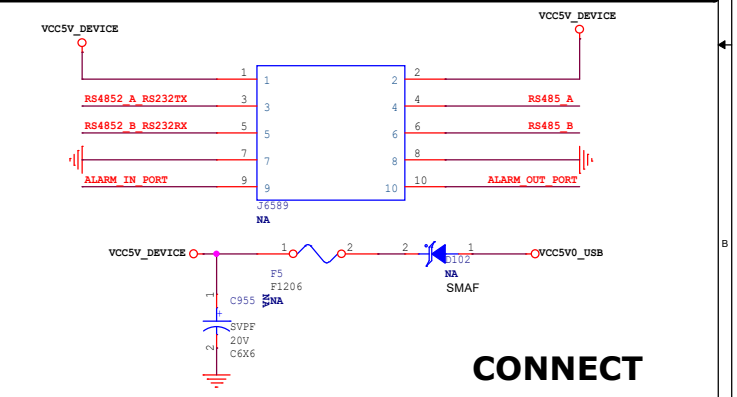


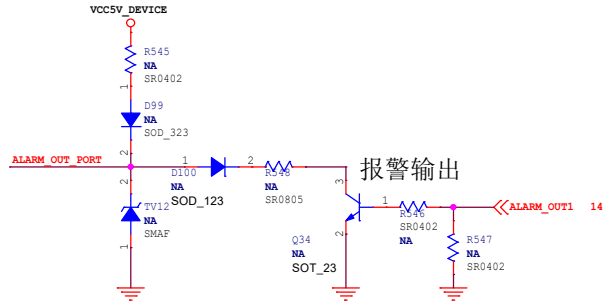
HINLINK			
Project:	H88K_V3.1	HINLINK	
File:	36.KEY_Array		
Date:	Tuesday, June 25, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	36 of 43

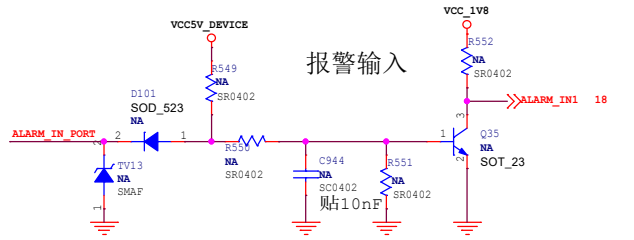


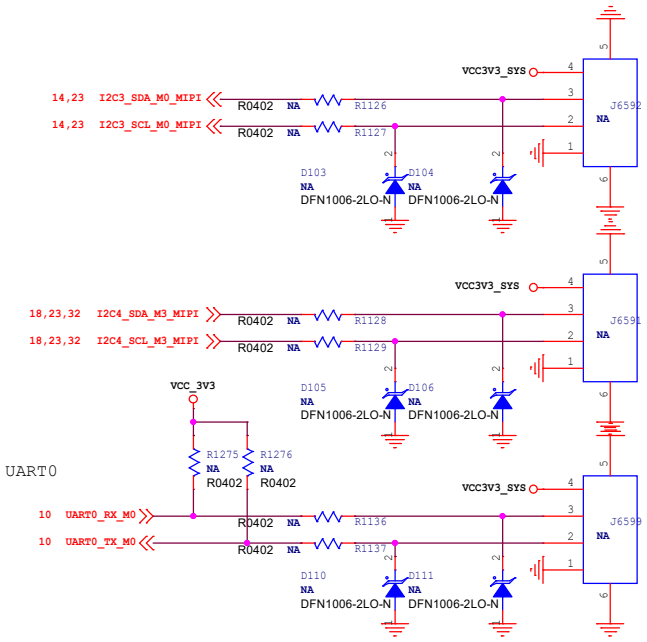


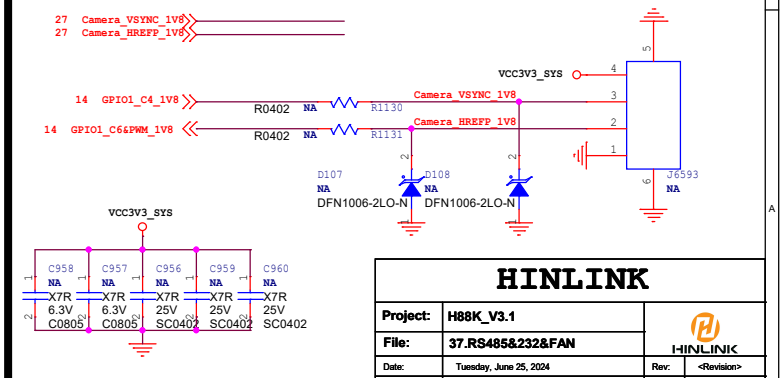




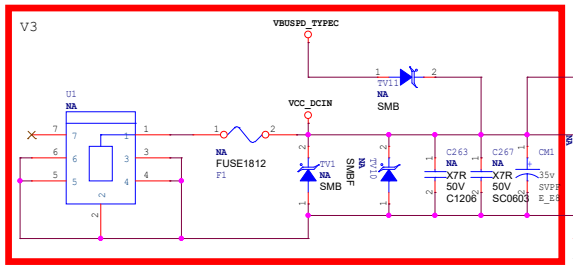




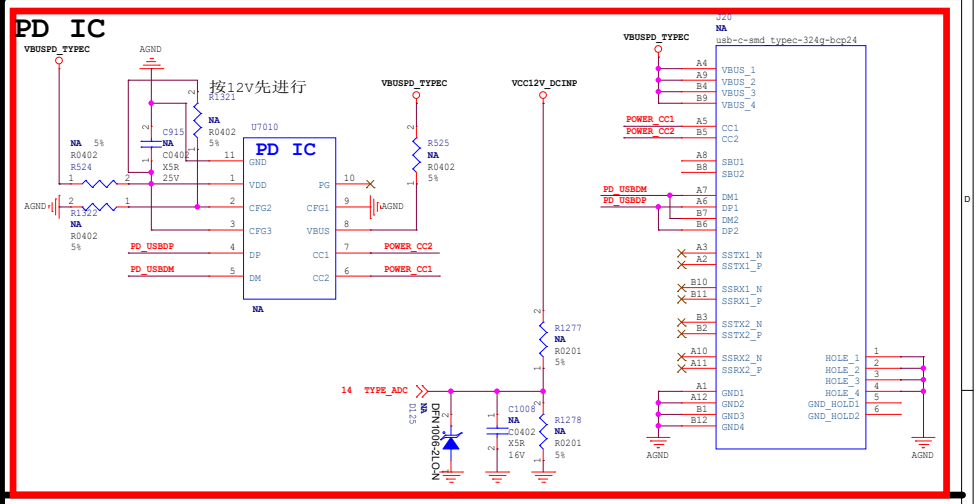




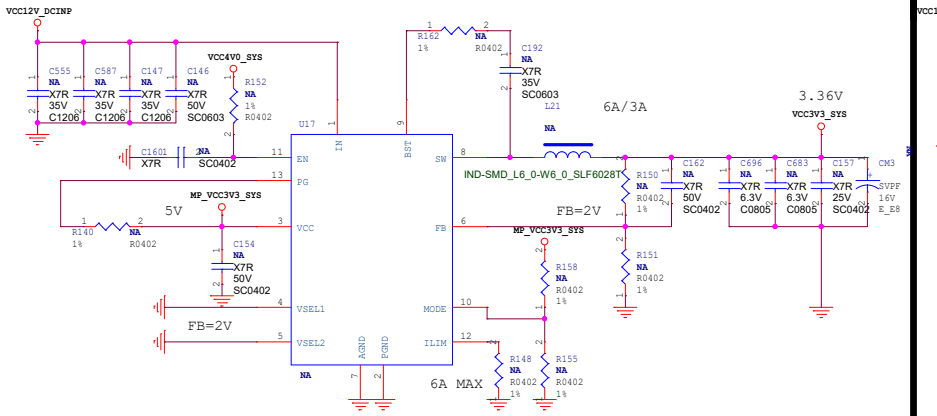
HINLINK			
Project:	H88K_V3.1		
File:	37.RS485&232&FAN		
Date:	Tuesday, June 25, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	37 of 43



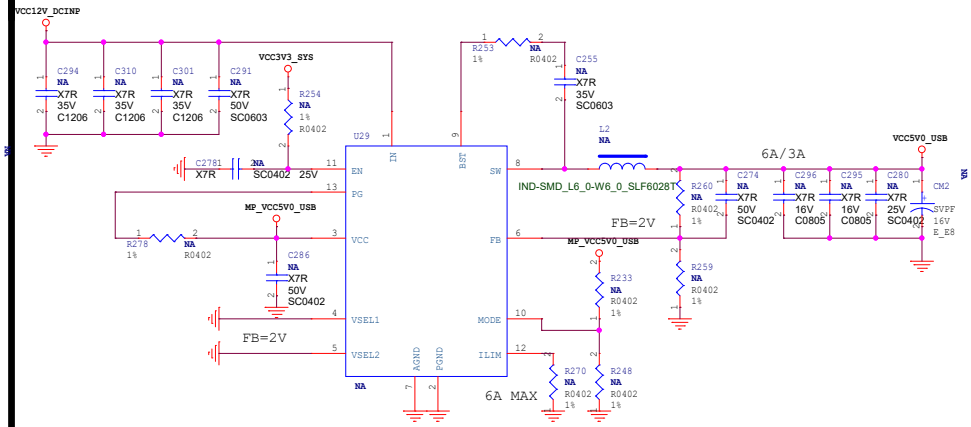
12-24V/3A DCIN



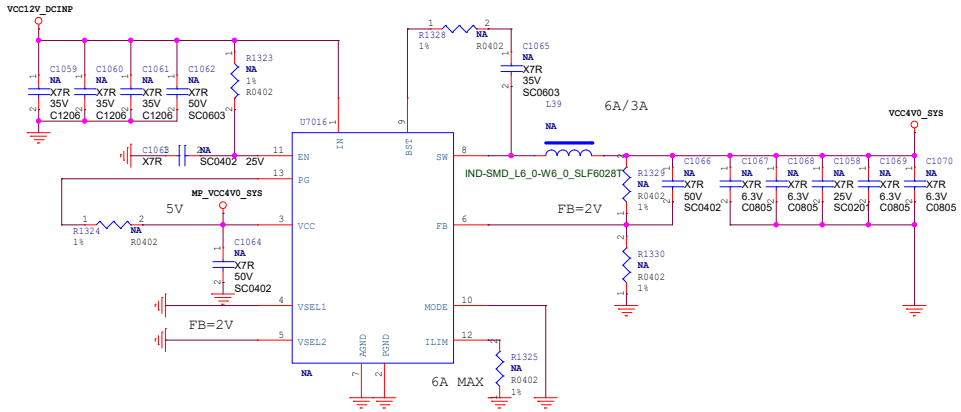
VCC3V3_SYS



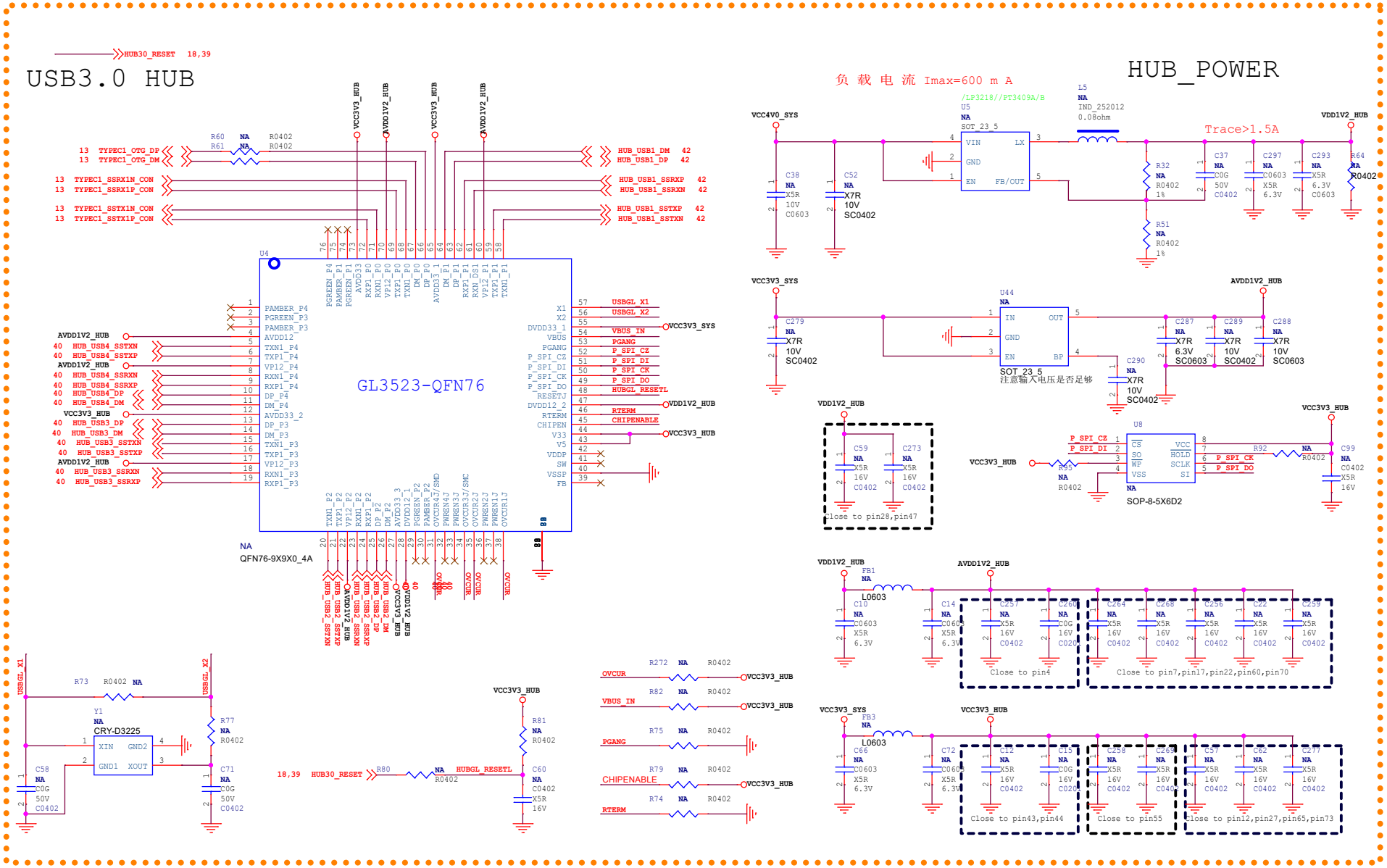
VCC_5V0 FOR USB+5V Device



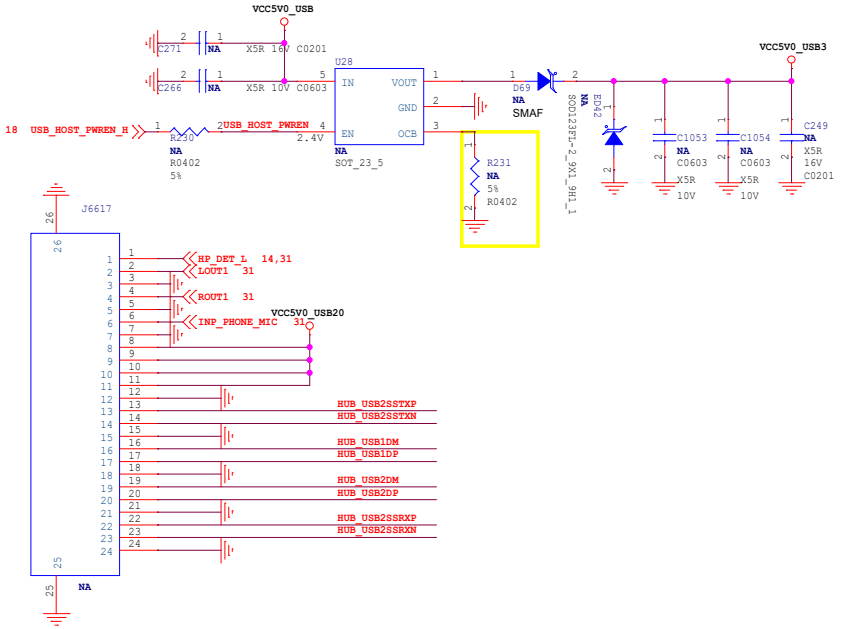
VCC4V0_SYS



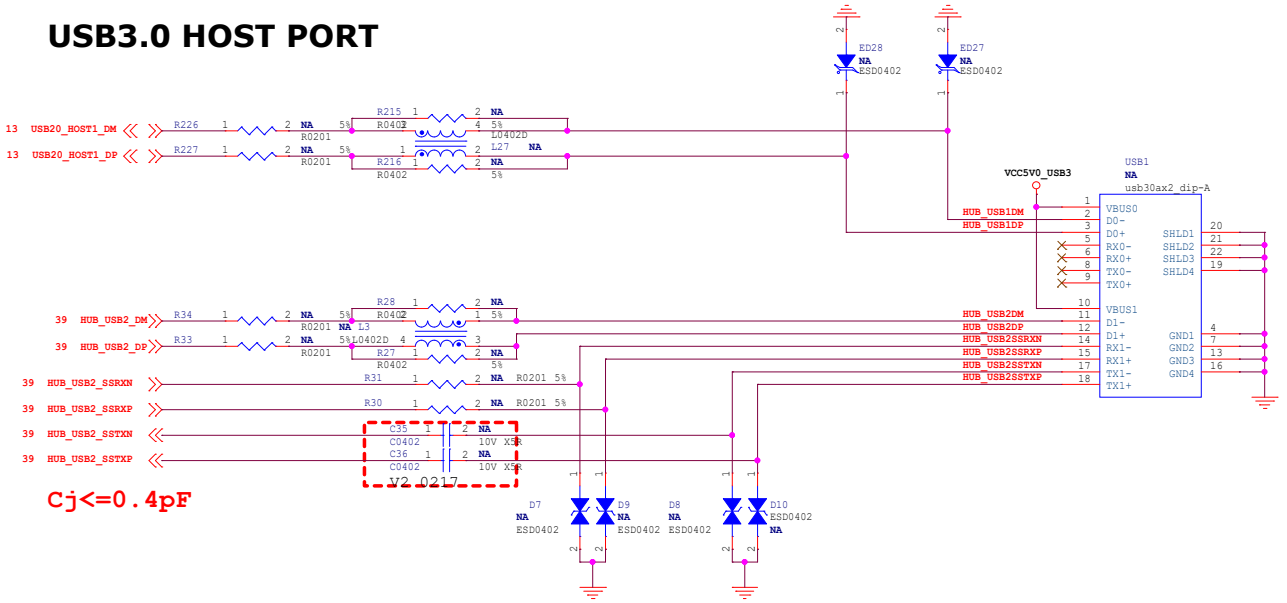
HINLINK		
Project:	H88K_V3.1	HINLINK
File:	38.POWER_IN	
Date:	Tuesday, June 25, 2024	Rev: <Revision>
Designer:	<designer>	Sheet: 38 of 43

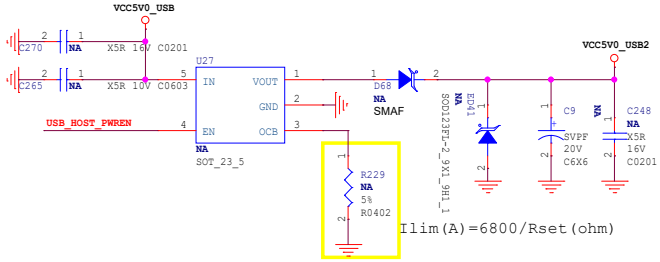


HINLINK			
Project:	H88K_V3.1		
File:	39.USB_HUB		
Date:	Tuesday, June 25, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	39 of 43

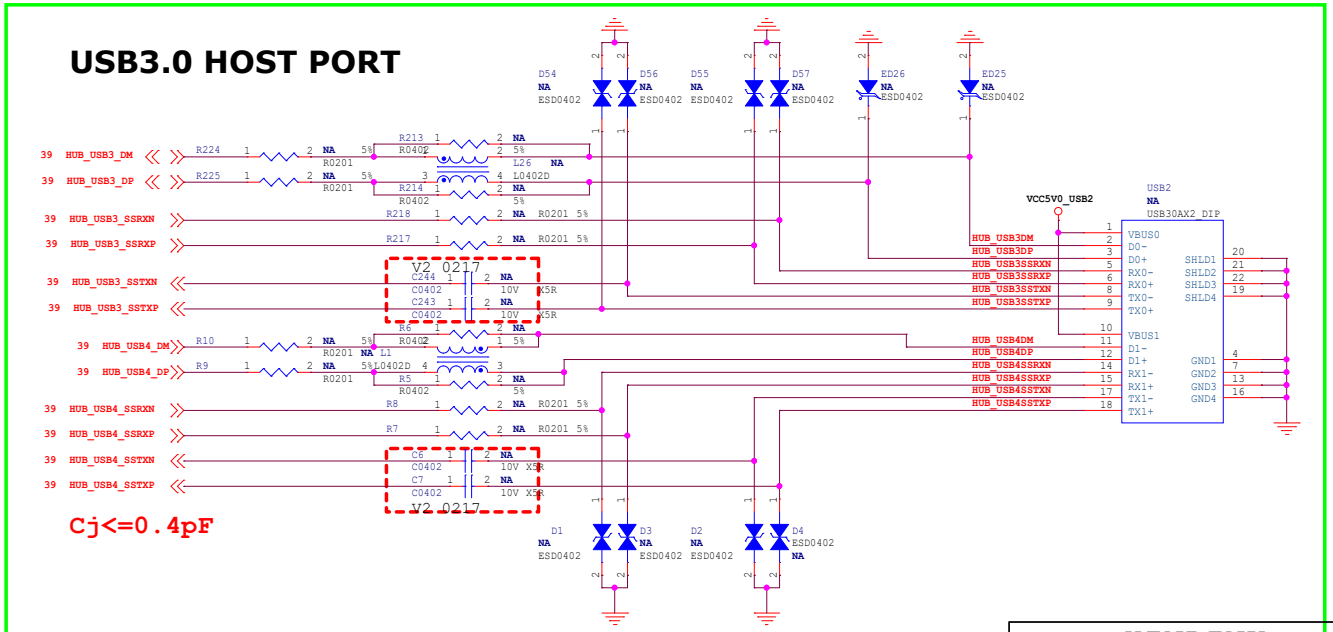


USB3.0 HOST PORT





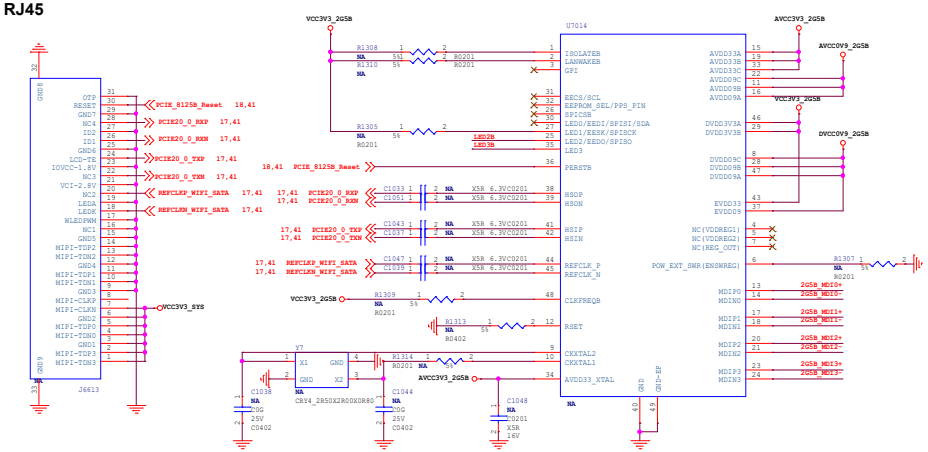
USB3.0 HOST PORT

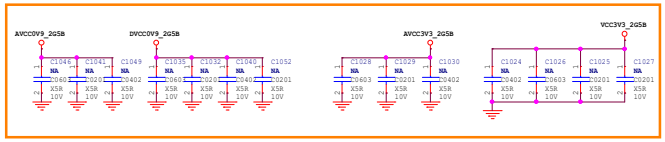


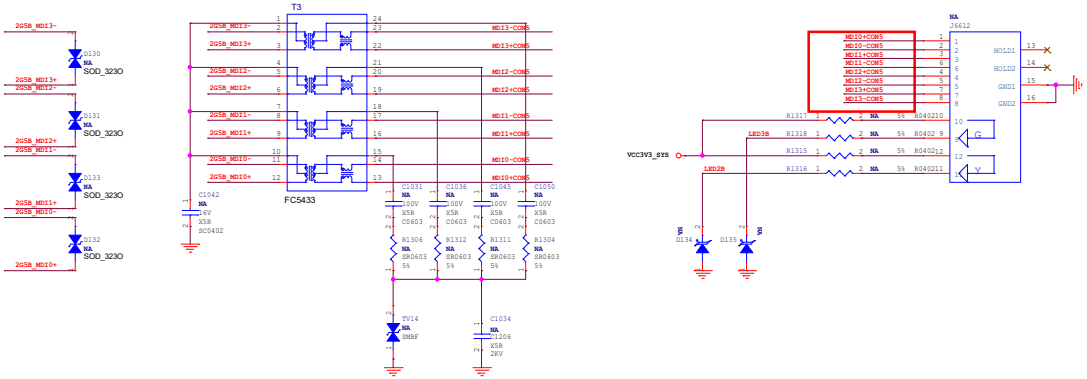
HINLINK

Project:	H88K_V3.1	HINLINK	
File:	40.USB_Port		
Date:	Tuesday, June 25, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	40 of 43

PCIE TO RJ45

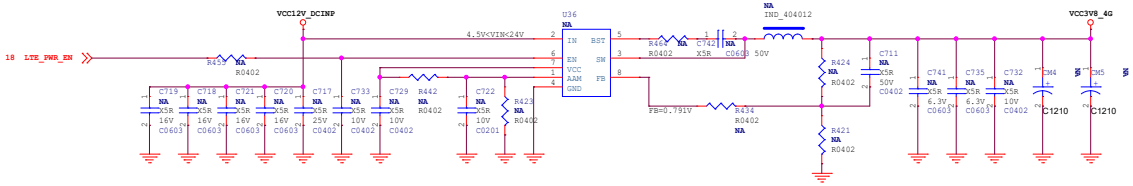




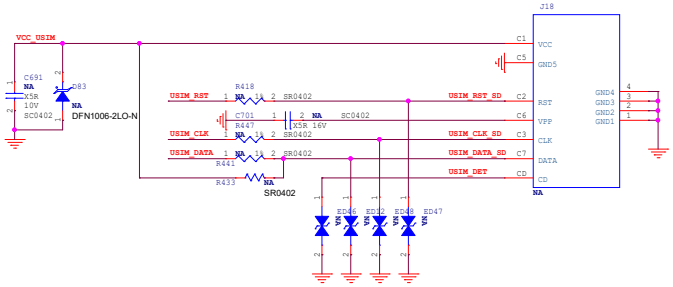


HINLINK		
Project:	H88K_V3.1	
File:	41.RTL8125B	HINLINK
Date:	Tuesday, June 25, 2024	Rev: <Revision>
Designer:	<designer>	Sheet: 41 of 43

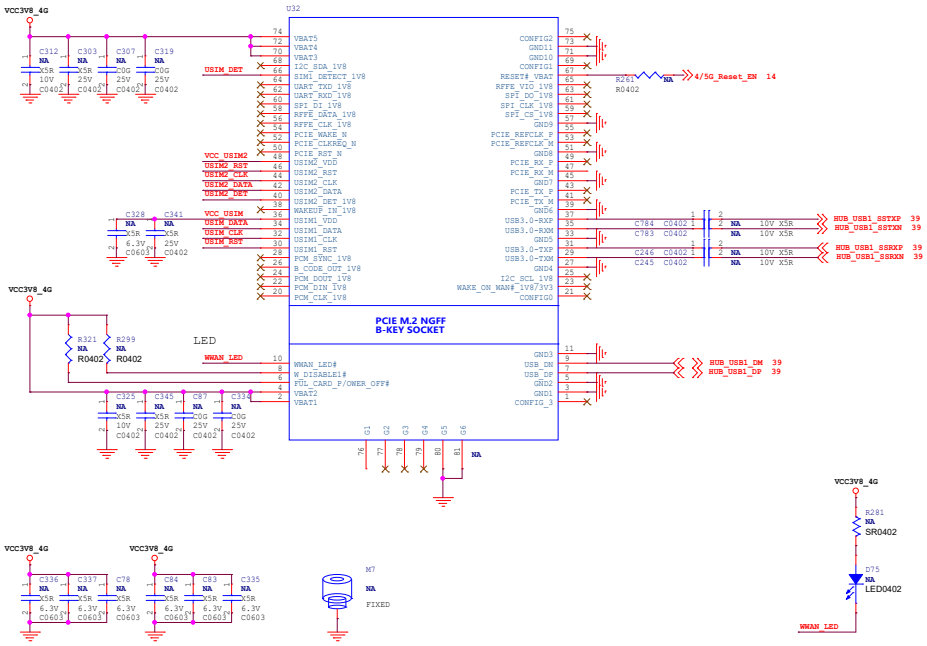
12V->3.8V



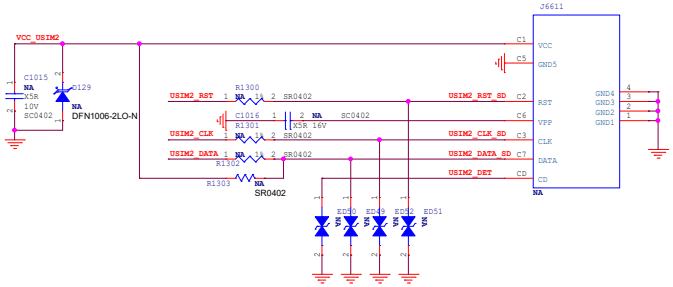
4G/5G SIM1 CARD



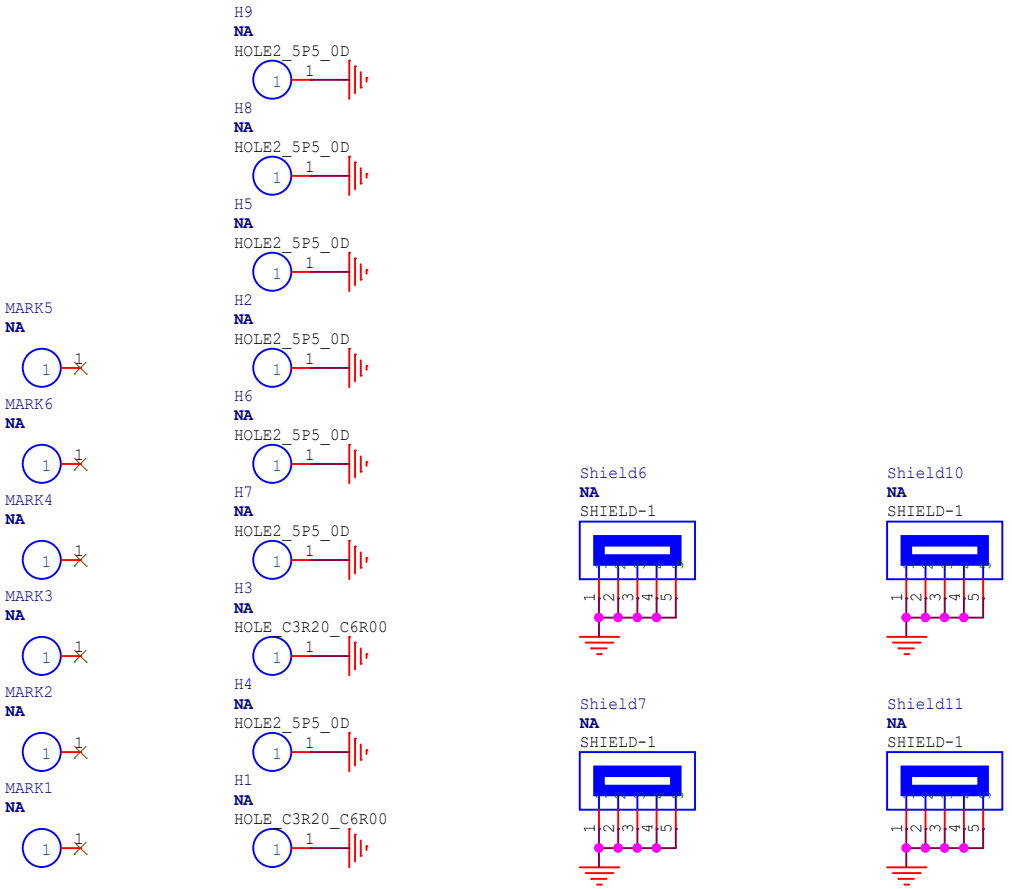
M2_NGFF-4G/5G



4G/5G SIM2 CARD



HINLINK			
Project:	H88K_V3.1		
File:	42.4G/5G-MODULE		
Date:	Tuesday, June 25, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	42 of 43



HINLINK			
Project:	H88K_V3.1	HINLINK	
File:	43.MARK/HOLE		
Date:	Tuesday, June 25, 2024	Rev:	<Revision>
Designer:	<designer>	Sheet:	43 of 43